Warszawskie Zakłady Urządzeń Informatyki
MERAMAT

SYSTEM MERA 9150

Podręcznik serwisowy

1

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1

FOREWORD

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This issue of the manual supercedes all copies issued prior to June 1976 containing unmarked issue pages. The manual has been completely revised and additional sections added. Section 12 is not issued and reserved for future insertion. Each page of the manual now bears an issue number as a basis for future updates.

Each revised or additional page issued in future will be marked up with a subsequent issue number and listed in the accompanying amendment sheet. This action will enable all manual holders to keep track of the status of their manuals.

Each revised page is intended to replace the page of the previous issue (i.e. issue-2 page will replace issue-1 and so on).

All manual holders are requested to destroy the old copies on receiving the new manual.

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AMENDMENTS

AMENDMENT SHEET

The following pages of this manual are revised to Issue 2. Synchronous Line Controller Section 12 and additional pages to Memory Section 2 and Diagnostic Section 9 are added. Pages 3–21 to 3–29 are deleted.

Section 1, page 1–15 Disc Program and Section 4, page 4–51 Mag Tape Program are obsolete and therefore deleted from this manual.

Revised Page Numbers

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12–1 TO 12–13 — ADDED

20/1/1977

AMENDMENT SHEET

This amendment reference number is A–01. It consists of additional pages that are being incorporated in Sections 4 and 6 of the manual. It also includes one update page (i.e. page 4–1) the issue which is raised from 1 to 2. A new section 8A is added in Binder 1 of the manual.

These pages are:–

Page No.	Issue No.
4 – 1	2
4 – 64	1
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8A – 1	1
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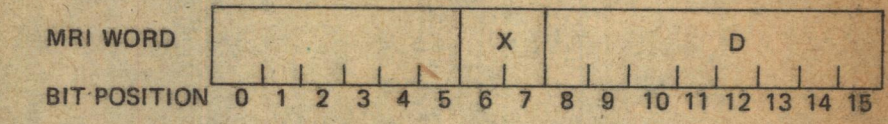
CPU

INDEX ADDRESSING

Index addressing is accomplished by coding 2 numbers into the Memory Reference Instruction. An Index (X) Mode and a Displacement (D).



The bits contained in bit positions 6 and 7 of the Memory Reference Instruction (MRI) specify the Index (X) Mode, and those contained in bit positions 8 thru 15 specify the Displacement (D).

The four values for X instruct the CPU to fetch a 15-bit number (address).

In the CPU there are 5 accessible temporary storage registers. Four of these storage registers are 16-bit accumulators and the fifth is the 15-bit program counter (PC). The PC is 15 bits since any address can be expressed with 15 bits. NOTE: The PC is only accessable from the front panel (not under program control).

The Displacement (D) is an 8-bit number which can take on the following octal values:

UNSIGNED:	000	thru	377
SIGNED:	-200	thru	+177

To calculate the effective address use

$$E = (X) + D$$

Where the notation (X) refers to the fetched 15-bit number. If X = 0, (X) = 00000 and E will actually be the value of D. If X = 1, then (X) equals the 15-bit contents of PC or present address.

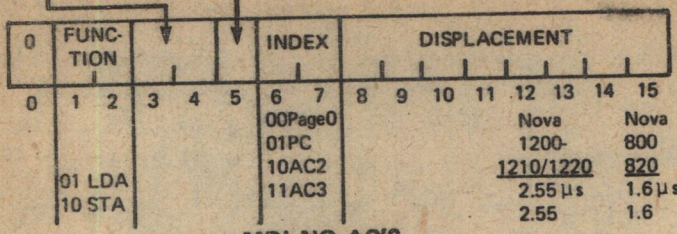
If X	Then (X) is	The Possible Values for D are	The Possible Effective Addresses (E) are
00	00000	000 thru 377	00000 thru 00377 (Page 0)
01	(PC)	-200 thru +177	(Present location -200) thru (Present location +177)
10	(AC2)	-200 thru +177	[(AC2) -200] thru [(AC2) +177]
11	(AC3)	-200 thru +177	[(AC3) -200] thru [(AC3) +177]

MEMORY REFERENCE

INSTRUCTIONS

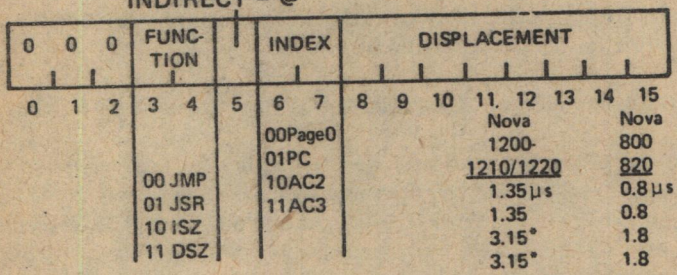
MRI WITH AC'S

AC ADDRESS INDIRECT = @



MRI NO AC'S

INDIRECT = @



*Add 1.35 µs if skip occurs

In the following descriptions AC is the accumulator (if any) specified by the instruction, and E represents the effective address calculated from the address information given by the instruction.

LDA — Load Accumulator. Load the contents of location E into AC.

STA — Store Accumulator. Store the contents of AC in location E. (AC not changed)

ISZ — Increment and Skip if Zero. Add 1 to the contents of location E and place the result back in E. Skip the next instruction in sequence if the result is zero.

DSZ — Decrement and Skip if Zero. Subtract 1 from the contents of location E and place the result back in E. Skip the next instruction in sequence if the result is zero.

JMP — Jump. Load E into PC. Take the next instruction from location E and continue sequential operation from there.

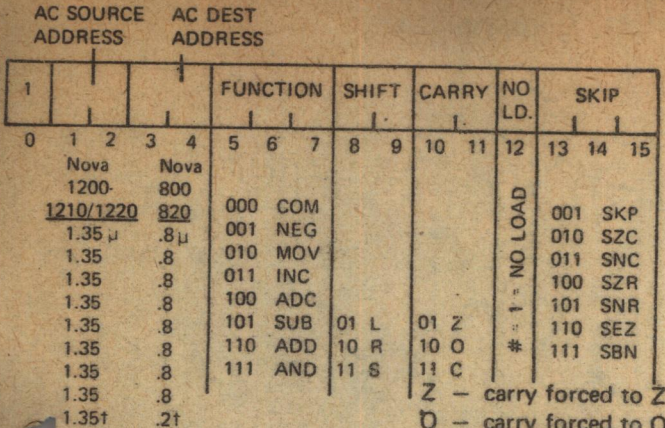
JSR — Jump and Save Return. Load E into PC. Load into AC3 the address of the location following the JSR instruction. Take the next instruction from location E and continue sequential operation from there.

Automatic Incrementing
@ 00020 - 00027

Automatic Decrementing
@ 00030 - 00037

The contents of the location indirectly addressed is incremented before it becomes the address.

ALC – Arithmetic, logical & Carry instructions



†Add if skip occurs.

An ALC instructions is identified by bit 0 being set

COM — Complement. Place the (logical) complement of the word from ACS in ACD.

NEG — Negate. Place the twos complement of the number from ACS into ACD. Complement Carry if ACS contains zero. (Forming the twos complement of zero generates a carry, because complementing zero produces a word containing all 1s. and adding 1 to that produces all zeros again, plus a carry.)

MOV — Move. Place the contents of ACS in ACD.

INC — Increment. Add 1 to the number from ACS and place it in ACD. If the result is 2^{16}, complement Carry.

ADC — Add Complement. Add the (logical) complement of the number from ACS to the number from ACD and place the result in ACD. If the original ACD $>$ ACS, complement Carry.

SUB — Subtract. Add the twos complement of the number from ACS to the number from ACD and place the result in ACD. If the original ACD $\geqslant$ ACS, complement Carry.

ADD — Add. Add the number from ACS to the number from ACD and place the result in ACD. If the result is $\geqslant 2^{16}$, complement Carry.

AND — And. Place the logical AND function of the word from ACS and the word from ACD in ACD.

SKP — Always Skip.

SZC — Skip on Zero Carry.

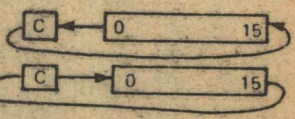
SNC — Skip on Nonzero Carry.

SZR — Skip on Zero Result.

SNR — Skip on Nonzero Result.

SEZ — Skip if Either Carry or Result is Zero.

SBN — Skip if Both Carry and Result are Nonzero.



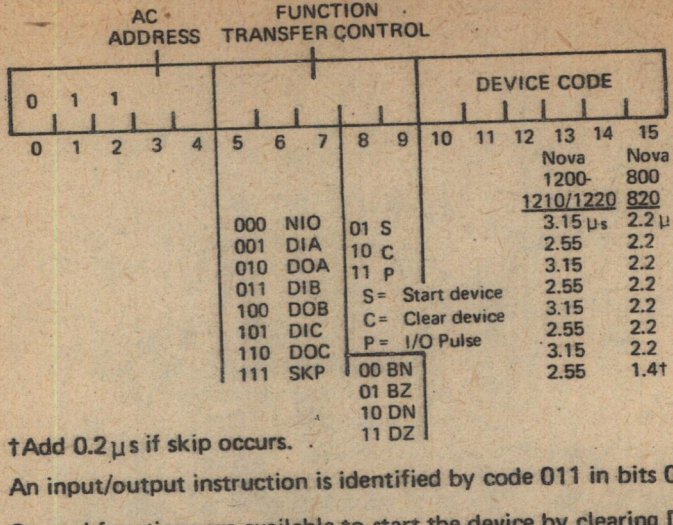
L — A left shift

R — A right shift

S — SWAP – Bit o through 7 are swapped with bits 8 through 15. The carry bit is not affected.

INPUT/OUTPUT

INSTRUCTIONS



†Add 0.2 µs if skip occurs.

An input/output instruction is identified by code 011 in bits 0, 1 & 2

Control functions are available to start the device by clearing Done and setting Busy; to clear both Busy and Done, idling the device; and to generate a special Pulse whose effect, if any, depends on the device.

DIA	Data In A
DOA	Data Out A
DIB	Data in B
DOB	Data Out B
DIC	Data In C
DOC	Data Out C
NIO	No IO Transfer. Perform the specified control function.
SKPBN	Skip if Busy is Nonzero.
SKPBZ	Skip if Busy is Zero.
SKPDN	Skip if Done is Nonzero.
SKPDZ	Skip if Done is Zero.

DZ = is it reset
DN = is it set (done)

SPECIAL INSTRUCTIONS

INTEN NIOS CPU 060177
Interrupt Enable.

INTDS NIOC CPU 060277
Interrupt Disable.

READS DIA AC, CPU 060477
Read Switches. Read the contents of the console data switches into AC.

INTA DIB AC, CPU 061477
Interrupt Acknowledge. Place in AC the device code of the first device on the bus that is requesting an interrupt (("first" means physically closest to the processor on the bus).

MSKO DOB AC, CPU 062077
Mask Out. Set up the interrupt Disarm flags in the devices according to the mask in AC. For this purpose each device is connected to a given da line, and its flag is set or cleared as the corresponding bit in the mask is 1

DIC 0, CPU 062477

Clear IO Devices. Clear the control flip-flops, including Busy, Done, Interrupt, and interrupt request, in all devices connected to the bus.

IORST DICC 0, CPU 062677

IO Reset. Clear all IO devices and disarm all interrupts.

HALT DOC 0, CPU 063077

Halt the Processor.

SKPBN CPU

Skip if Interrupt On is Nonzero.

SKPBZ CPU

Skip if Interrupt On is Zero.

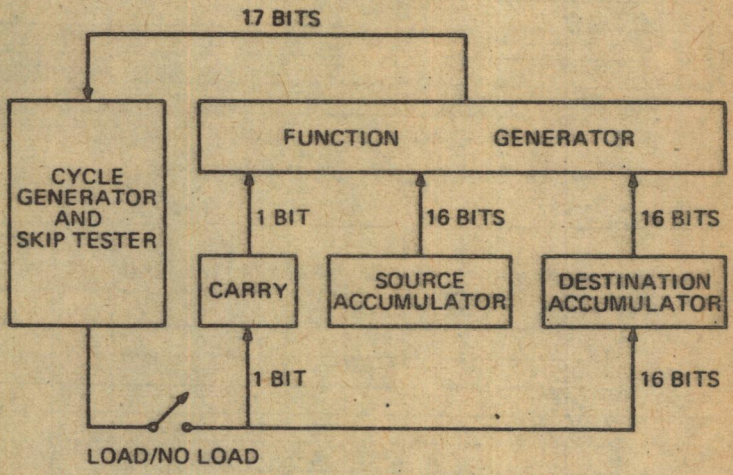
SKPDN CPU

Skip if Power Failure is Nonzero.

SKPDZ CPU

Skip if Power Failure is Zero.

THE ARITHMETIC UNIT



Each ALC instruction specifies one or two accumulators to supply operands to the function generator, which performs the function specified by the instruction. The function generator also produces a carry bit whose value depends upon three quantities: a base value specified by the instruction, the function performed, and the result obtained. The base value may be derived from the Carry flag, or the instruction may specify an independent value.

The 17-bit output of the function generator, comprising the carry bit and the 16-bit function result, goes to the shifter. The 17-bit result can be rotated one place right or left, or the two 8-bit halves of the 16-bit function result can be swapped without affecting the carry bit. The 17-bit shifter output can be tested for a skip and the skip sensor can test whether the carry bit or the rest of the 17-bit word is or is not equal to zero. The 17-bit shifted word is loaded into Carry and one of the accumulators selected by the instruction. Note: loading is not necessary. An instruction can perform a complicated arithmetic and shifting operation and test the result for a skip without affecting Carry or any accumulator.

ALC CARRY

Prior To Instruction	IR		Overflow Occurred?	Carry At Completion
	Bit 10	Bit 11		
Carry Reset	0	0	No	Reset
Carry Reset	0	0	Yes	Set
Carry Set	0	0	No	Set
Carry Set	0	0	Yes	Reset
Carry Reset	0	1	No	Reset
Carry Reset	0	1	Yes	Set
Carry Set	0	1	No	Reset
Carry Set	0	1	Yes	Set
Carry Reset	1	0	No	Set
Carry Reset	1	0	Yes	Reset
Carry Set	1	0	No	Set
Carry Set	1	0	Yes	Reset
Carry Reset	1	1	No	Set
Carry Reset	1	1	Yes	Reset
Carry Set	1	1	No	Reset
Carry Set	1	1	Yes	Set

CONTROL SWITCH DECODING TO THE IR

Console Instruction		IR0	IR1	IR2	IR3	IR4	IR5	IR6	IR7	IR8 To 15
AC DEP.	AC0	0	0	1	0	0	0	1	1	0
	AC1	0	0	1	0	1	0	1	1	0
	AC2	0	0	1	1	0	0	1	1	0
	AC3	0	0	1	1	1	0	1	1	0
AC EXAM.	AC0	0	1	1	0	0	1	1	1	0
	AC1	0	1	1	0	1	1	1	1	0
	AC2	0	1	1	1	0	1	1	1	0
	AC3	0	1	1	1	1	1	1	1	0
Deposit		1	1	0	1	1	1	0	1	0
Deposit Next		1	1	0	1	1	1	0	0	0
Examine		1	1	1	1	1	0	0	1	0
Examine Next		1	1	1	1	1	1	0	0	0
Memory Step		1	1	1	1	1	1	1	1	0
Instruction Step		1	1	1	1	1	1	1	1	0
Program Load		1	1	1	1	1	1	0	1	0
Start		1	1	1	1	1	0	1	1	0

ACD + ACEX

ACD

Dep. + Dep. Next

AC Select on ACD + ACEX

Data taken from switches

Next state key M

Deposit next + examine next

Always false on k...

COLD START PROGRAM

Device	Loc	Data
Diablo Disk	000176 000177	060132 000177
7 Channel Tape Transport	000176 000177	060123 000177
9 Channel 800 BPI Tape Transport	000176 000177	060122 000177
9 Channel 1600 BPI [illegible]e Transport	000176 000177	060120 000177

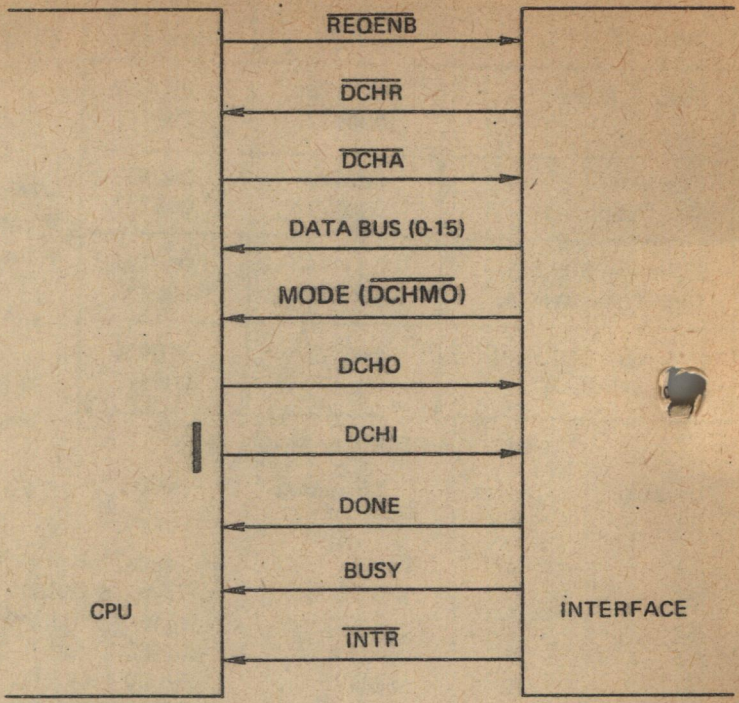
Load appropriate program and start at location 176.

DEVICE CODES & MASK BITS

Int Mask Bit	Device Code	Mnemonic	Device
14	10	TTI	Teletype Input
15	11	TTO	Teletype Output
12	17	LPT	Line or Serial Printer
10	20	MTA	9/1600 Tape
10	22	MTA	9/800 Tape
10	23	MTA	7/800 7/556 Tape
9	31	DSK	3 Board Disk Controller
9	32	DSK	Single Board Disk Controller
9	33	DSK	Second Single Board Disk Cont.
8	40	REC	Communications Receiver (IBM)
8	41	XMT	Communications Transmitter (IBM)
8	44	REC	Communications Receiver (ICL)
8	45	XMT	Communications Transmitter (ICL)
—	60		Scanner
—	61		Scanner (Terminal Channel)
[illegible]	64	RTC	Real Time Clock
—	77	CPU	Central Processing Unit
7	16	CDR	Card Reader
	21		REI Interface
	37	OCR	ODP Interface
1	*	ICA	Input Core Address OVERFLOW
3	*	IER	Input Error (Scanner)
11	12	PTR	Paper Tape Reader
13	13	PTP	Paper Tape Punch

* Device code as associated with MSKO instruction

DATA CHANNEL SIGNALS



SEQUENCE:

1. REQENB to I/O
2. DCHR to CPU
3. DCHA to I/O

4a. Main Memory Address on Data Bus to CPU

b. Mode Bits to CPU (see Table)

5. Data on Data Bus Direction Determined by Type of Operation
6. DCHO to Interface

A. Overflow Line Applies on to Add Memory and Increment Mode

B. Done, Busy and INTR Same as Normal I/O

MODE BIT TABLE

DCHMO	Function
H	Output from memory
L	Input to memory

INTERFACE

	Active	To	Pin
CLEAR	H	D	A50
DATA0	L	B	B62
DATA1	L	B	B65
DATA2	L	B	B82
DATA3	L	B	B73
DATA4	L	B	B61
DATA5	L	B	B57
DATA6	L	B	B95
DATA7	L	B	B55
DATA8	L	B	B60
DATA9	L	B	B63
DATA10	L	B	B75
DATA11	L	B	B58
DATA12	L	B	B59
DATA13	L	B	B64
DATA14	L	B	B56
DATA15	L	B	B66
DATIA	H	D	A44
DATIB	H	D	A42
DATIC	H	D	A54 ①
DATOA	H	D	A58
DATOB	H	D	A56
DATOC	H	D	A48
DCHA	L	D	A60
DCHI	H	D	B37
DCHMO	L	P	B17 ②
DCHMI	L	P	B21 ① ②
DCHO	H	D	B33

	Active	To	Pin
DCHP IN	L	D	A94 ③
DCHP OUT	L	D	A93 ③
DCHR	L	P	B35
DSO	L	D	A72
DSI	L	D	A68
DS2	L	D	A66
DS3	L	D	A46
DS4	L	D	A62
DS5	L	D	A64
INTA	H	D	A40 ③
INTP IN	L	D	A96 ③
INTP OUT	L	D	A95
INTR	L	P	B29
IOPLS	H	D	A74 ①
IORST	H	D	A70
MSKO	L	D	A38
OVFLO	H	D	B39 ①
RQENB	L	D	B41
SELB	L	P	A82
SELD	L	P	A80
STRT	H	D	A52
COLD STRT	H	D	A49

L = Low, H = High } active

B = Both directions

D = Device from processor

P = Processor from device

① Not used by disk controller.

② See table for mode bits, pg. 1–7.

③ If board removed, jumper -- In sig. from CPU or prev. device -- Out sig. to next device.

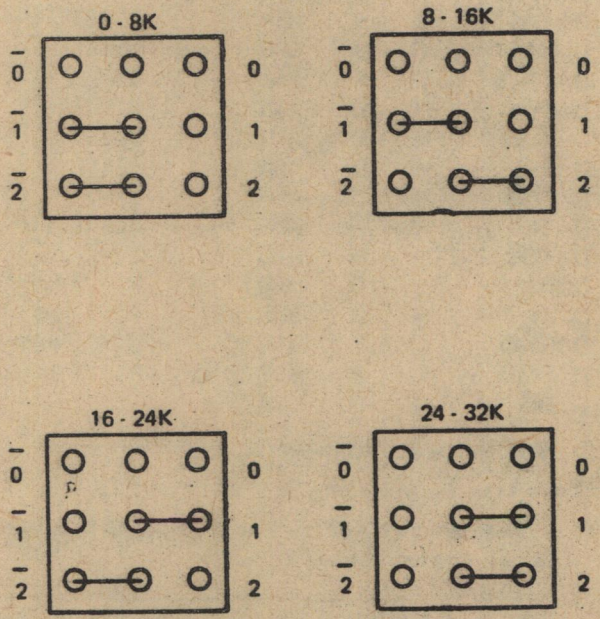
Slots	Pin No.	Volts	Power Supply
2–9	A6,B81	–5	Lower
1–7	A3,A4, B3,B4,A97,98,B97,98	+5	Lower
2–12	A10,B84	+15mem	Lower
8–17	A3,A4, B3,B4,A97,98,B97,98	+5	Upper
13–17	A3,A4, B3,B4	+5	Upper
10–17	A6,B81	–5	Upper
Not Used		–15	Lower

VOLTAGE MAP

The Processor

1. Clears Interrupt ON
2. Saves PC in Location 0
3. Simulates JMP@1 Contents of location 1 can contain a direct or indirect address

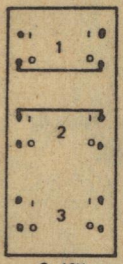
MEMORY SELECT ADDRESS JUMPER
NEW 8K MEMORIES



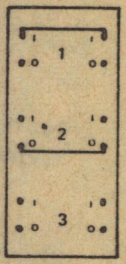
MEMORY ADDRESS SELECT JUMPERS (CONT.)

OLD 8K MEMORIES

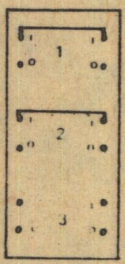
0-8K



8-16K

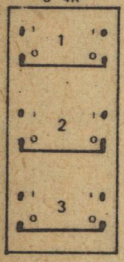


16-24K

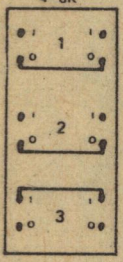


24-32K

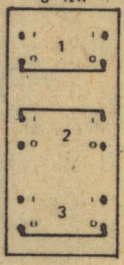
4K MEMORY BOARDS (Two Bay Systems)



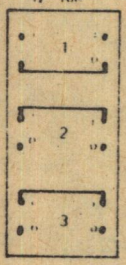
0-4K



4-8K



8-12K



12-16K

16-20K

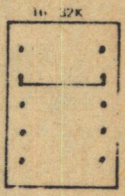
20-24K

24-28K

28-32K

16K MEMORIES

0-16K


16-32K

16K MEMORIES (FAST)

0-16K

16-32K

May also be addressed as 8K memories.

0-8K	link 5-12 and 3-14	16-24K	6-11 3-14
8-16K	5-12 4-13	24-32K	6-11 4-13

SUBJECT: The ILLS of Inserting CPU Boards into the Wrong Slot!

When the CPU P.C. Board is inserted into the wrong slot, disaster may resu
The return inhibit signals for the memory is connected to the logic inside t
CPU Board. This results in +15 being connected to much of the logic, with
resulting destruction.

If you should be so fortunate as to have this happen, below is a troublesho
aid which can be used to locate the bad chips.

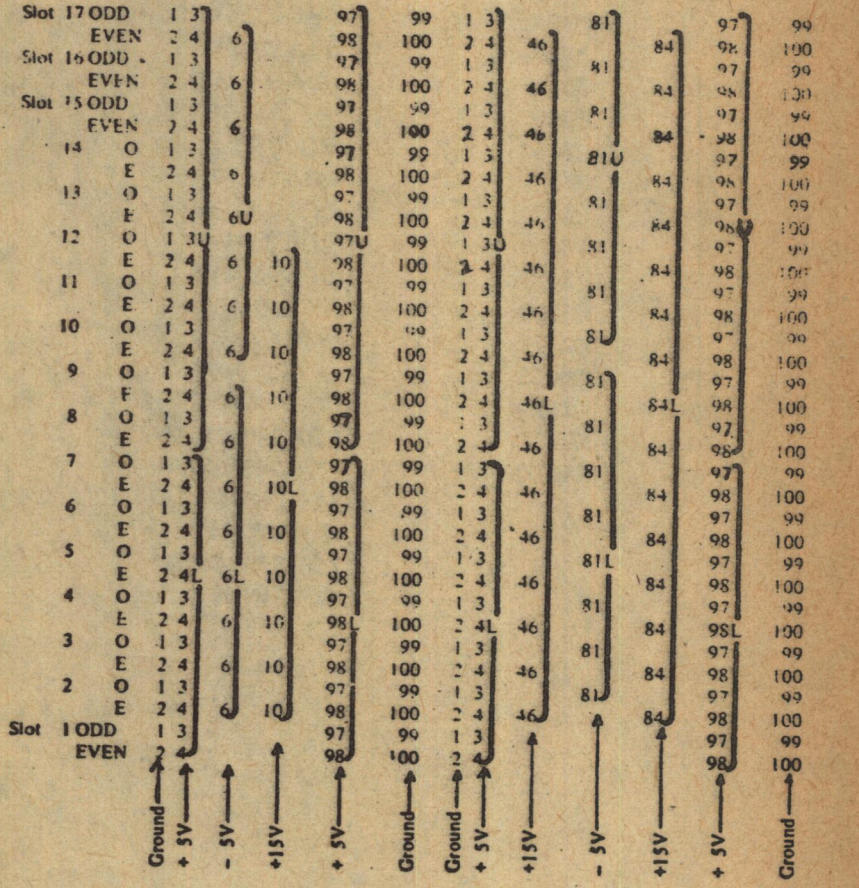
GOOD LUCK!

Signal Name	Rev Level Less Than E D116E Location	N[illegible]1200
Power Fail	12, 16, 124	86
Mem Ok	59, 51, 11, 49	62, 83, 125, 111
Exec	79, 57	73, 52
Fetch	27, 12, 62, 114	94, 45, 75, 89
Carry	10, 62	76, 6, 77
1STP	15	24
PL	98, 83, 61	41, 43, 87
CON+1S[illegible]+MSTP	61	3
CON Reg	61	3
CON Data	118	3, 4, 6
CON 1STR	95	1, 2, 5
most probably bad chip locations	15, 27, 59, 61, 79, 95 115, 124	86, 62, 73, 94 24, 3, 4, 5[illegible]

MOTHER BOARD VOLTAGE CHECK POINTS

-15V FROM LOWER SUPPLY NOT USED

U = From Upper Supply
L = From Lower Supply



WRITE PATTERN TO TAPE FOR SCOPING – A. Sharmer

```
700     060477      ;DIA O CPU
701     034410      ;LDA 3 +711
702     024410      ;LDA 1 +712
703     124400      ;NEG 1 1
704     041400      ;STA 0 +0 3
705     175400      ;INC 3 3
706     125404      ;INC 1 1 SZR
707     000775      ;JMP + 704
710     000403      ;JMP + 713
711     001000      ADDRESS
712     000100      # WORDS/RECORD
713     034776      ;LDA 3 + 711
714     030776      ;LDA 2 + 712
715     150520      ;           NEG ZL 2, 2
716     151220      ;MOVZR 2 2
717     024407      ;LDA 1 + 726
720     0650XX      ;DOA 1 MTA + 1
721     0760XX      ;DOB 3 MTA + 1
722     0731XX      ;DOCS 2 MTA + 1
723     0635XX      ;SKPBZ MTA + 1
724     000777      ;JMP + 723
725     000753      ; + 753 ; JMP + 700
726     0000XX      COMMAND 50/150 = WRITE
1000    002401      LOAD PROGRAM 2
1001    000700      PATCH MEMORY
                    SET SWITCHES = 14
                    START
                    SET SWITCHES =7
                    CONTINUE
```

To Write/Read to Disk (Manually Position to Cyl 202)

Loc	Instruction			
0	NIO	C	31	;CLR STATUS
1	LDA	0	OP CODE	;SET
2	DOA	0	31	;OP CODE
3	LDA	0	CORE ADR;	
4	DOB	0	31	;CORE ADR
5	LDA	0	BLK ADR	;
6	DOC	S 0	31	;BLK ADR+START
7	SKP	BZ	31	;WAIT TILL
10	JMP	.	-1	;END OP
11	DIA	0	31	;EXAMINE
12	JMP	.	+1	;STATUS
13	JMP	.	$-13_{(8)}$	:LOOP
14	OP CODE: ...			
15	CORE ADR: 100			CONSTANTS
16	BLK ADR: 062400			

Loc	Instruction	
0	060231	
1	020413	
2	061031	
3	020412	
4	062031	
5	020411	
6	063131	
7	063531	
10	000777	
11	060431	
12	000401	If Halt desired
13	000765	Store 063077
14	010000	Write Sector
	004000	Rd Sector
15	000100	
16	062400	

Write Pattern to Memory

0/ 063077 – Halt
1/ 074477 – Read Switches in AC 3
2/ 060101 – NIOS
3/ 046020 – STA
4/ 000775 – JMP-3
20/ 000021 – All Memory, except 1--20
Sync on NIO

ADDRESS→PERIPH/RETURN ADDRESS/COMPARE

```
1000/   060477 DIA 0, CPU      Reads sw to AC0
1001/   062032 DOB 0, 32       Load Address your periph
1002/   126400 SUB 1, 1        Clear AC1 ?
1003/   065432 DIB 1, 32       Read Address
1004/   106414 SUB 0, 1,SZR    Compare
1005/   063077 HLT
1006/   000772 JMP. -6         Loop program
```

Examine 1000/
Set switches your address pattern.
Continue
If program halts, examine AC0 and AC1
AC0 = word attempted/AC1 = word received

This program allows you to check the data buss between the CPU and a peripheral controller for picked or dropped bits. Scope for marginal bits. Can also check the Controller Address Register.

Disk SEEK 4 CYL and RESTORE

```
AC0 = 4000/  AC1 =  1000
                    61032 DOA,0,32
                    67132 DOCS,1,32
                    63532
                      777 JMP. -1
                    62677 IORST
                    63532
                      777 JMP. -1
                      771 JMP. -7
```

CPU HARDWARE DESCRIPTION

The CPU is a 16 bit, 2's complement machine.

Transfer to and from the memory is in parallel. All data transfers within the processor are in 4 bit bytes.

All the logic is contained on one logic board.

Instructions

There are 3 classes:—

1.	Memory Reference	MRI
2.	Input/Output	I/O
3.	Arithmetic and Logic	ALC

Major States

There are 8 Major States which define the type of memory function.

1.	FETCH.	Fetches next word for use as an instruction.
2.	DEFER.	Uses next word from memory as a new address (indirect addressing).
3.	EXECUTE.	This occurs after fetch when the next word from memory is to be used as the operand. (Programmed I/O instructions also set execute but the memory does not run).
4.	P.I.	Program Interrupt.
5.	DCH.	Data channel transfer between I/O and Memory (DMA).
6.	KEY	Occurs when a manual function from the console is requested. No memory cycle.
7.	KEYM	Occurs when a manual function from the console is requested. e.g. examine.
8.	Dummy	Occurs when a machine stop is pending and skip interrogation is required.

Timing

The basic clock is 13.333 MHZ which is divided by two to give a 150nS clock time period.

Each 4 clock pulses constitutes one of two timing states TS0 and TS3).

There are at least two timing states for every major state.

In addition to the TS pulses there are 3 timing generators.

1. Processor timing generator. PTG

   This is a two bit counter which together with TS gives PTGC. 1,2,5. and is used to time the 4 bits nibble transfers through the CPU.

2. Accumulator timing generator. ACTG

This is a two bit counter ACTGC, 1, which drives the accumulators. During the EFA portion of the fetch it is 1 clock period ahead of the PTG to allow for the one clock delay through the D and S buffers.

3. Memory timing generator. MTG

This is a four bit counter which forms the memory control signals. MTGO, 1,2,3.

Registers

The CPU register organisation is shown in the block diagram given on page 1-19. The information transfer paths shown by heavier lines are 16-bit and all others 4-bit transfer routes.

Accumulators AC0, 1,2,3.

There are 2 identical sets of four 16-bit registers. The two sets being called Destination (ACD) and Source (ACS) and contain the same information. This is so that the data can be fetched simultaneously from two accumulators and added or logically manipulated. In those instructions which specify two accumulators, the ACS Supplies one operand while the ACD supplies the second.

Accumulator Shift Buffer ACB

This is a 16-bit register which temporarily stores the result received from the Adder. Data is passed through the ACB to the Accumulators via the Shifter.

Shifter

This is a 4-bit logic which performs shift right or left during an ALC instruction.

Memory Buffer MBO

This buffer is a 16-bit register that operates in serial or parallel mode. It converts parallel data from memory into 4 bits for the processor and converts 4 bits from processor for 16-bit parallel transfer to the memory either as address or data.

Instruction Register IR & MBC

This 16-bit register is divided into two 8-bit parts IR and MBC. IR contains the op-code of current instruction being performed by the CPU. During a memory reference instruction MBC will contain the 8 Bit displacement.

Program Counter PC

This contains the 15 bit address of the next instruction to be fetched from memory. It is incremented by one each time an instruction is performed. The address word in PC is serially transferred to the MBO prior to each f[illegible].

D and S buffers

Contain the accumulator nibble being processed.

3:1 Multiplexer

This is a 4-bit logic which selects any one of the 3 inputs Adder, ACD, MBO nibbles required to be fed back to the MBO for storing it in memory.

Note: The 15-bit memory Address register MA and 16-bit Memory Buffer MB are both located in memory. MB drives the MEM bus when communicating with CPU and I/O bus when working with an I/O device. Similarly MA drives either MBO bus or I/O bus.

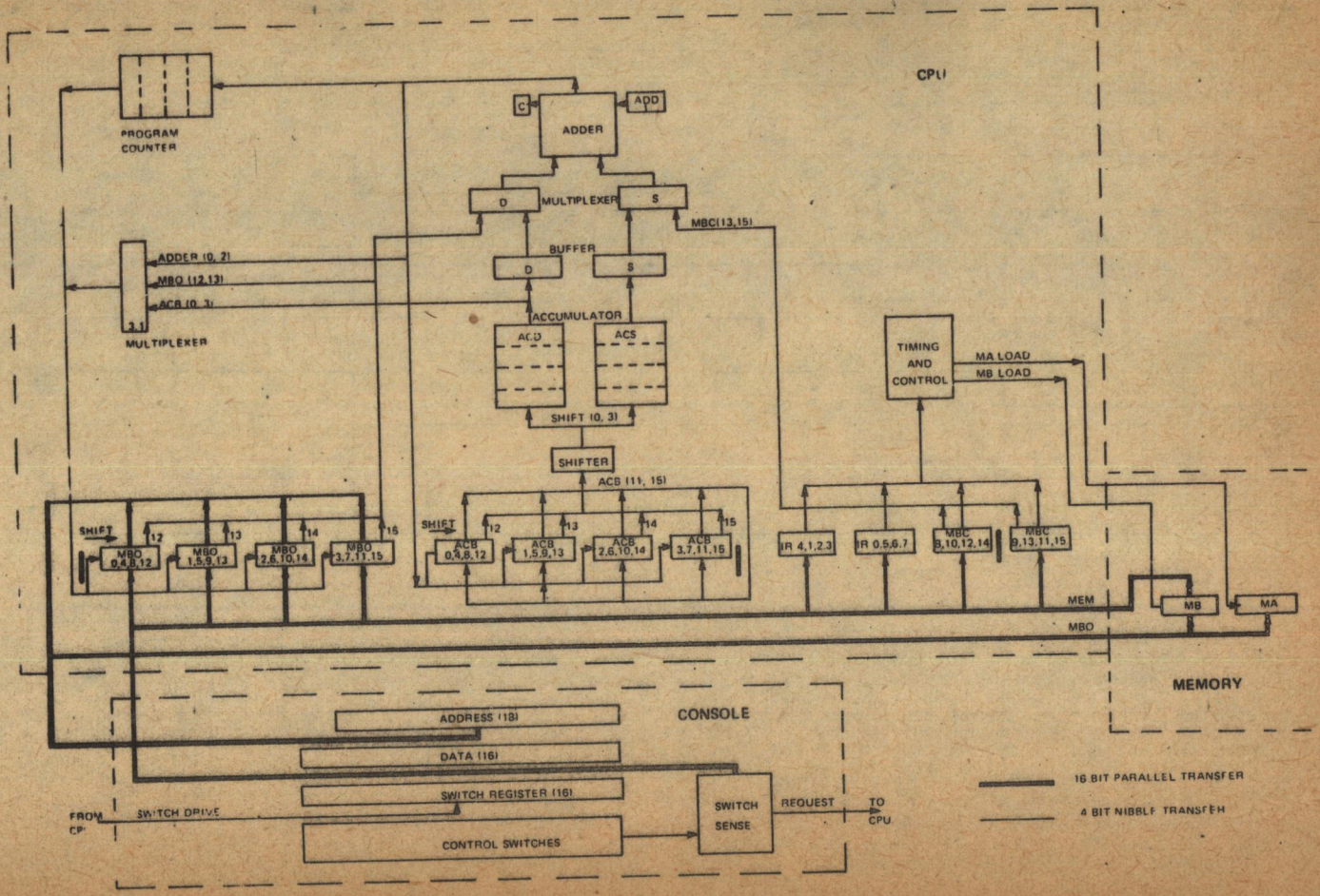
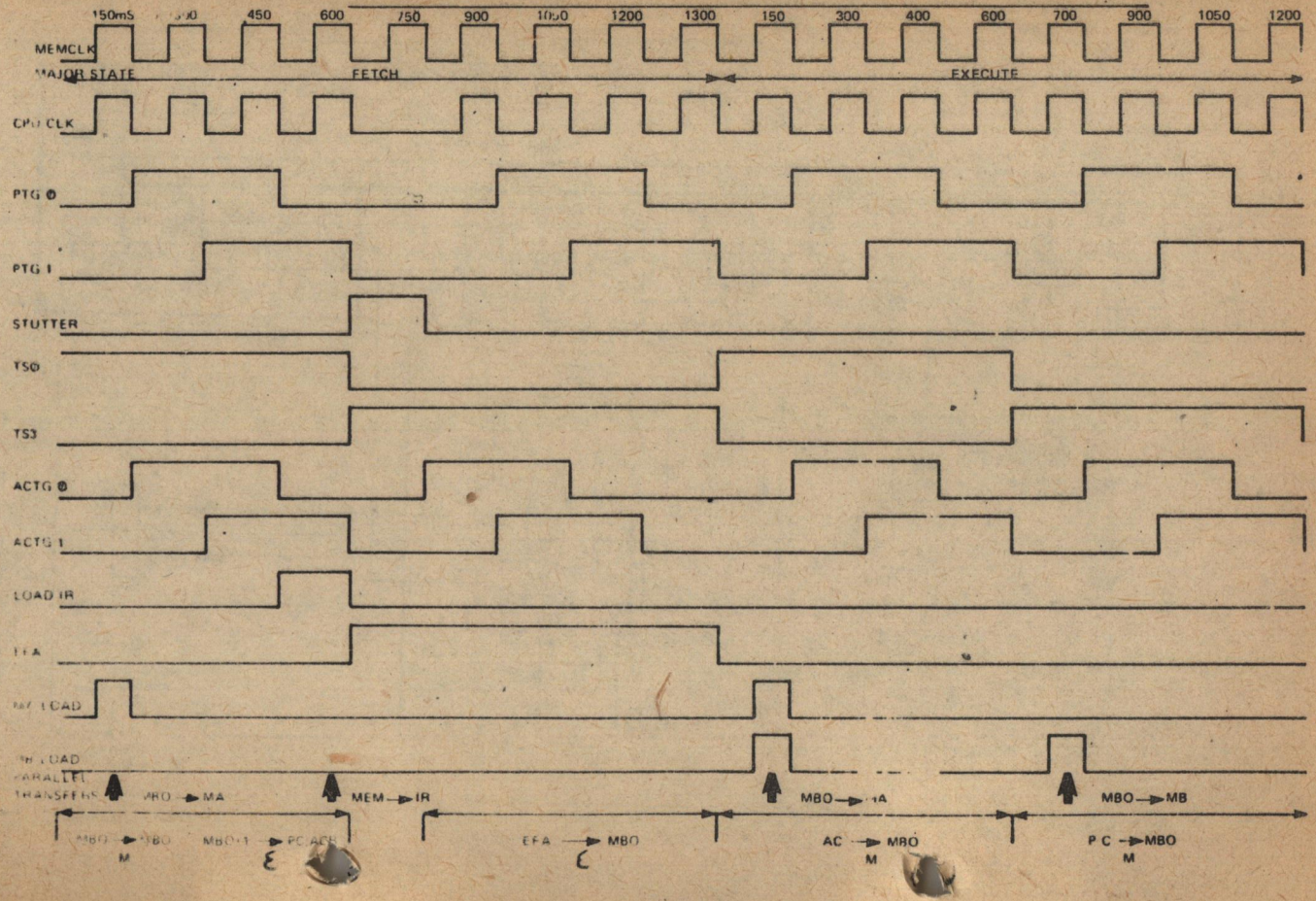
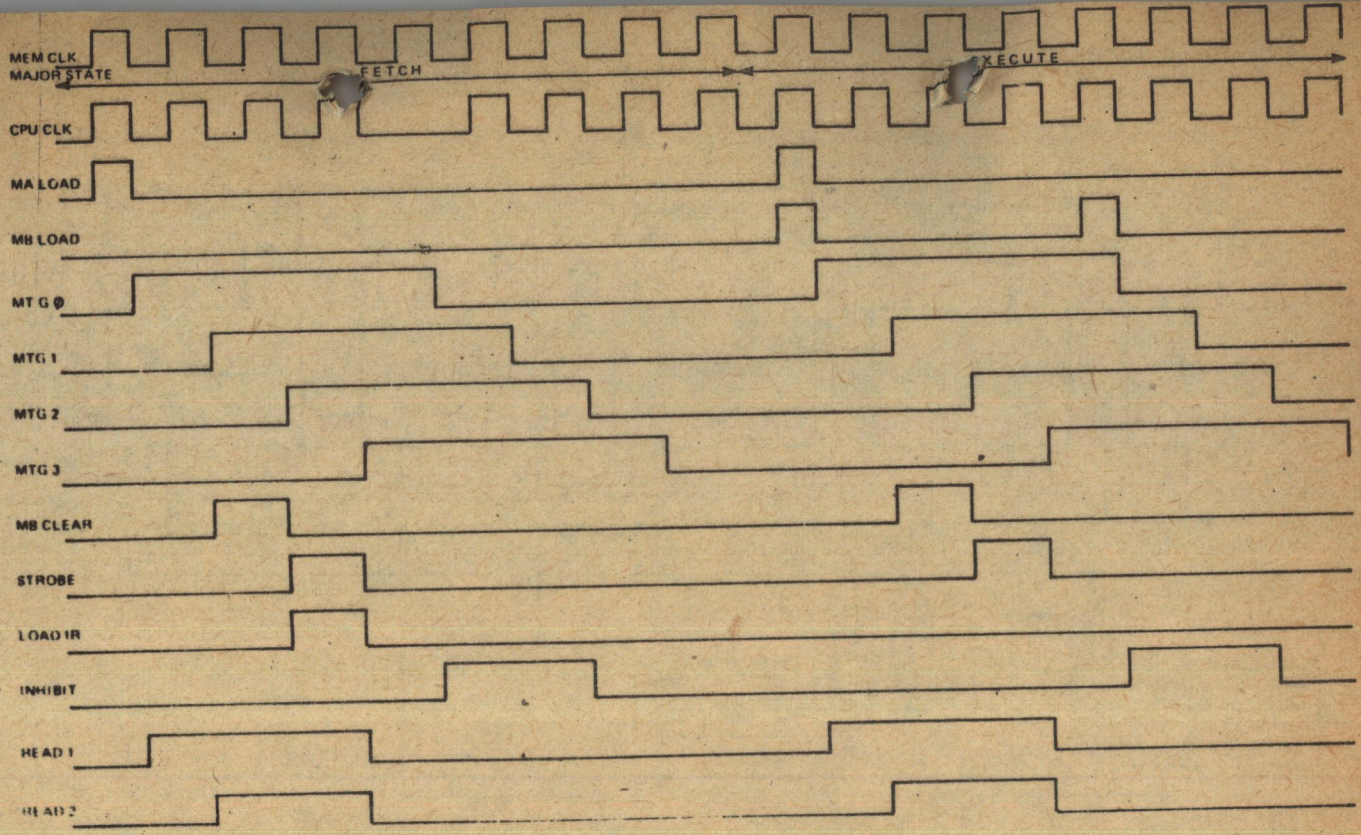
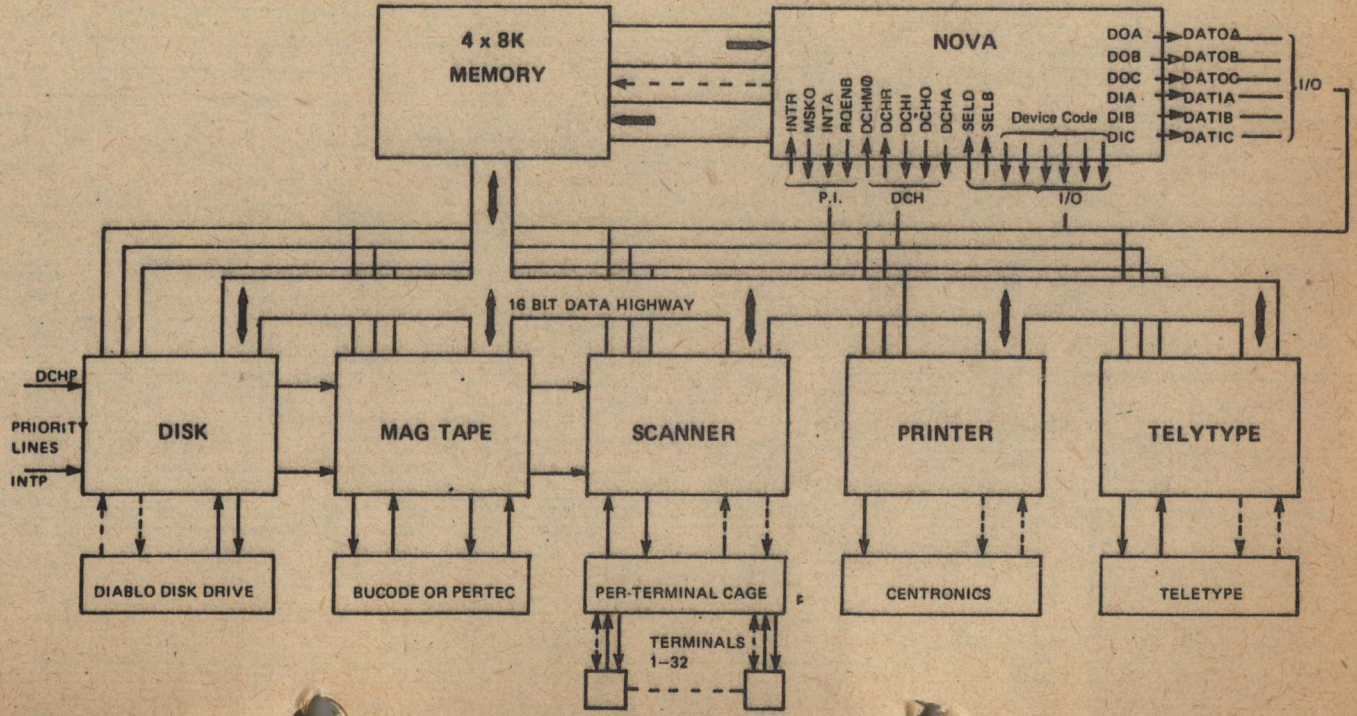

CPU
PROGRAM COUNTER
C
ADD
ADDER
D
MULTIPLEXER
S
MBC(13,15)
BUFFER
D
S
ADDER (0, 2)
MBO (12,13)
ACB (0, 3)
3,1
MULTIPLEXER
ACCUMULATOR
ACD
ACS
SHIFT (0, 3)
SHIFTER
ACB (11, 15)
TIMING AND CONTROL
MA LOAD
MB LOAD
SHIFT
MBO 0,4,8,12
MBO 1,5,9,13
MBO 2,6,10,14
MBO 3,7,11,15
ACB 0,4,8,12
ACB 1,5,9,13
ACB 2,6,10,14
ACB 3,7,11,15
IR 4,1,2,3
IR 0,5,6,7
MBC 8,10,12,14
MBC 9,13,11,15
MEM
MB
MA
MBO
MEMORY
CONSOLE
ADDRESS (18)
DATA (16)
SWITCH REGISTER (16)
CONTROL SWITCHES
FROM CP
SWITCH DRIVE
SWITCH SENSE
REQUEST
TO CPU
16 BIT PARALLEL TRANSFER
4 BIT NIBBLE TRANSFER

DIAGRAM SHOWING TIMING RELATIONSHIP BETWEEN THE NOVA COUNTERS, STA USED AS AN EXAMPLE




MEM CLK
MAJOR STATE
FETCH
EXECUTE
CPU CLK
MA LOAD
MB LOAD
MTG Ø
MTG 1
MTG 2
MTG 3
MB CLEAR
STROBE
LOAD IR
INHIBIT
READ 1
READ 2



SEECHECK SYSTEM DIAGRAM

COMPUTER OPERATION

The Computer may be operated either in manual mode under operator control or in auto mode under program control.

Manual Mode

When the computer is operated manually, the requests are entered using the front panel. Once a request is detected, the CPU enters a KEY major state which is immediately followed by RUN. RUN switches on CPU clocks and enables the CPU to execute the console request function in the KEY state. If the console request is an access to memory, the KEY state is immediately followed by a KEYM state.

Auto Mode

In this mode the CPU continually executes programmed instructions one after another while each instruction is taken from memory in a FETCH state. Note that before the CPU enters a FETCH state certain conditions such as a program interrupt or a data channel request or a stop, are checked. If none are present the CPU enters a FETCH state. In the FETCH state an instruction is fetched from a memory location specified by the program counter, placed in the IR register and decoded. If the decoded instruction is an ALC type instruction or JMP direct or JSR instruction, the CPU executes the instruction within the FETCH state. But when the instruction is an indirect (bits 5=1) memory reference, the FETCH state is immediately followed by a DEFER state. For a direct memory reference instruction (except JMP-JSR) or an I/O type instruction; the FETCH state is immediately followed by an Execute state.

SYSTEM DATA FLOW

Data flow between the CPU, Memory and I/O circuit boards is accomplished by means of MBO, MEM and I/O buses all which are 16-bit wide. Seecheck system diagram given on page 1-22 shows how these buses are interconnected. The MBO bus is driven by MBO located in the CPU and supplies data to the memory buffer (MB) and memory address register (MA) both located in memory. The same bus connects to the computer front panel. The MEM bus is driven by MB and supplies data to MBO and instruction register IR. The MEM bus also drives data lamps on the fron panel and supplies data to the CPU when the computer is operated manually. Both the MBO and MEM buses are unidirectional in that they supply data in one direction only. The I/O bus however, is a by-directional bus that links peripheral devices directly to the memory.

I/O SYSTEM

Data is transferred to a device (output) and from a device (input) via a 16 bit I/O highway (I/O bus). In conjunction with the data lines are a number of control lines both to and from the device.

There are 3 parts of the I/O system.

1. I/O transfer. Transfer is by a single instruction for each word transferred. Data is routed from or to an accumulator via the memory card.

2. DCH transfer. The Data channel mode has to be set up by means of a few single transfers. Once set up the data transfer is direct to or from memory, the time of each transfer being determined by the device.

3. P.I. Priority Interrupt is a means whereby a device can cause the CPU program to jump out of sequence and go to location zero.

1. I/O transfer

The I/O instructions DOA, 3, C and DIA, B, C send a signal down lines DATOA,B,C and DATIA,B,C. In conjunction with this signal are 6 bits which are decoded by each device. If the device code is true for a particular controller then in the case of DOA,B,C it uses the sign 1 DATOA,B,C to strobe the date from the I/O bus into its A, B or c buffer.

If the signal is a DATIA,B,C then the device puts the contents of the A, B or C buffer onto the I/O bus.

When the device code is decoded the device also gates the state of its Busy and Done flip-flops onto the SELB and SELD lines respectively.

On output the data is routed from the CPU Accumulator via the MBO, MBO lines, Memory buffer, I/O bus to the device.

On input, data is routed from the device via the I/O bus, Memory buffer, Mem lines, MBO to the Accumulator.

Although the data is routed through the memory card a memory cycle does not take place.

The state of busy and done define the current state of a device and must be interrogated with an I/O SKIP before setting up a device or transferring data.

2. DCH transfer

The data channel for a device is set up using the DOA,B,C instructions as appropriate.

The data channel has a serial priority system. Disk has highest priority and gates the priority line to the next device if it does not require a DCH transfer. The priority is Disk, Mag tape, Scanner, Printer, Teletype.

Request enable (RQENB) is sent from the CPU, any device requiring a transfer then sends DCH Request (DCHR) to the CPU. When the CPU sends DCH Acknowledge (DCHA), the device that has priority is then selected and that device puts the DCH Mode Ø line (DCHMØ) to a 1 or Ø depending on the type of transfer required (input or output). At the same time the device puts the memory address on the I/O bus.

When DCHA goes false the device takes the address off the I/O bus. After the memory read the CPU sends either DCH In (DCHI) or DCH Out (DCHO). For DCHI the device puts the data to be sent to memory on the I/O bus. For DCHO the device strobes the data off the I/O bus into its data buffer.

The control of the memory is at all times done by the CPU.

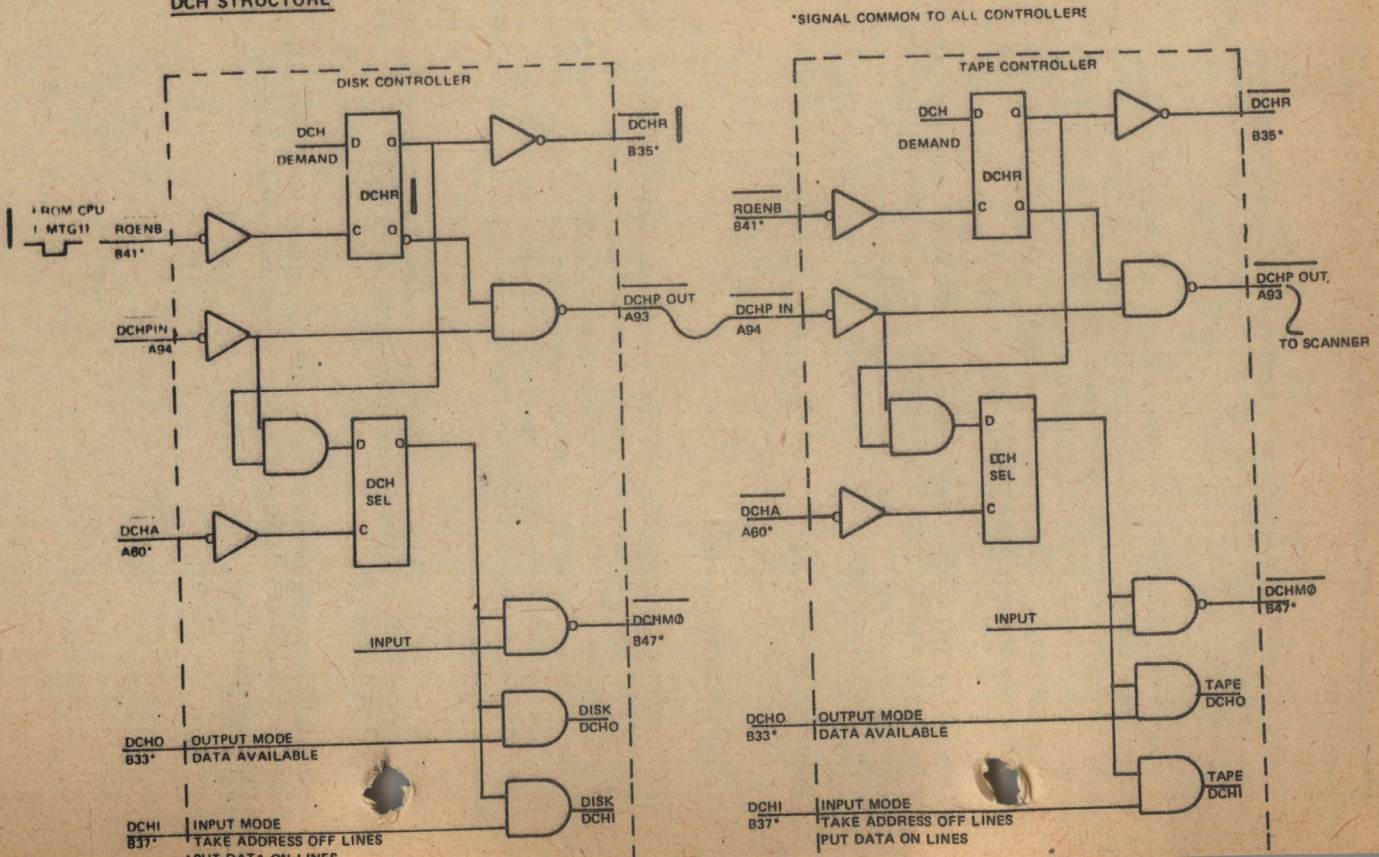
3. P.I. Priority Interrupt

The interrupt system has a similar Priority system to the data channel. The same RQENB signal is used for the interrupt system, and is used to set interrupt request. This causes the CPU to jump to location zero. The address (Program Counter) at which the interrupt occured is also saved in location zero. When an Interrupt Acknowledge (INTA) is sent from the CPU the device that has priority puts its device code on the I/O bus which is inputted to one of the accumulators.

The interrupt can be inhibited (masked) by the Mask Out line (MSKO). When this signal is seen by the device it uses its assigned bit on the I/O bus to set an interrupt disable F/F.

An interrupt is usually generated by Done which informs the CPU that the device has completed the last transfer (or block of transfers for DCH) and requires setting up again.

DCH STRUCTURE

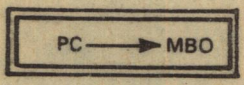


INSTRUCTION FLOW CHARTS

Page	FLOW CHART
1	FETCH
2	ALC
3	EFA
4	DEFER
5	EXECUTE
6	I/O FCOM
7	DCH
8	P.I.
9	CONSOLE REQUEST. KEY
10	KEYM

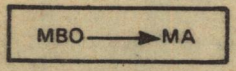
LEGEND

TYPE OF CYCLE



NIBBLE TRANSFER.

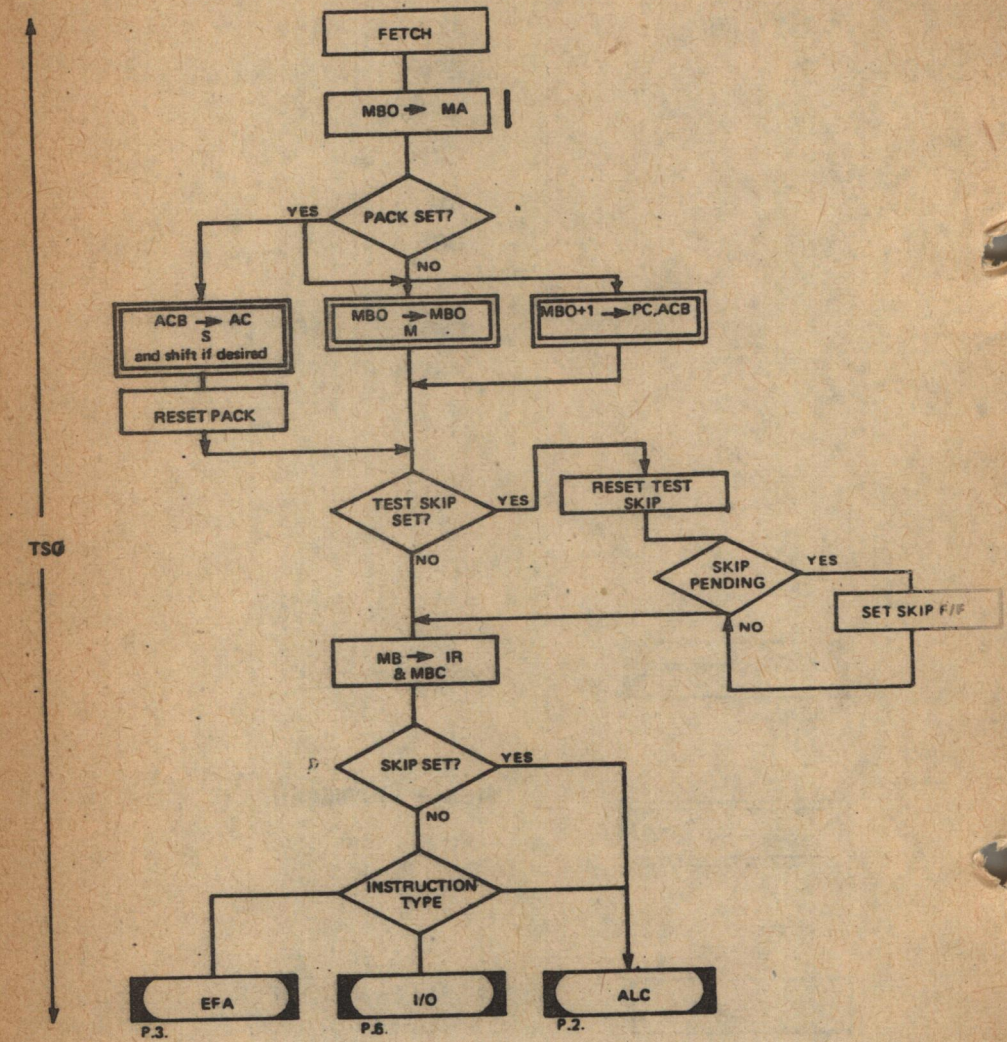
4 Bits at a time.
4 Clock Periods.

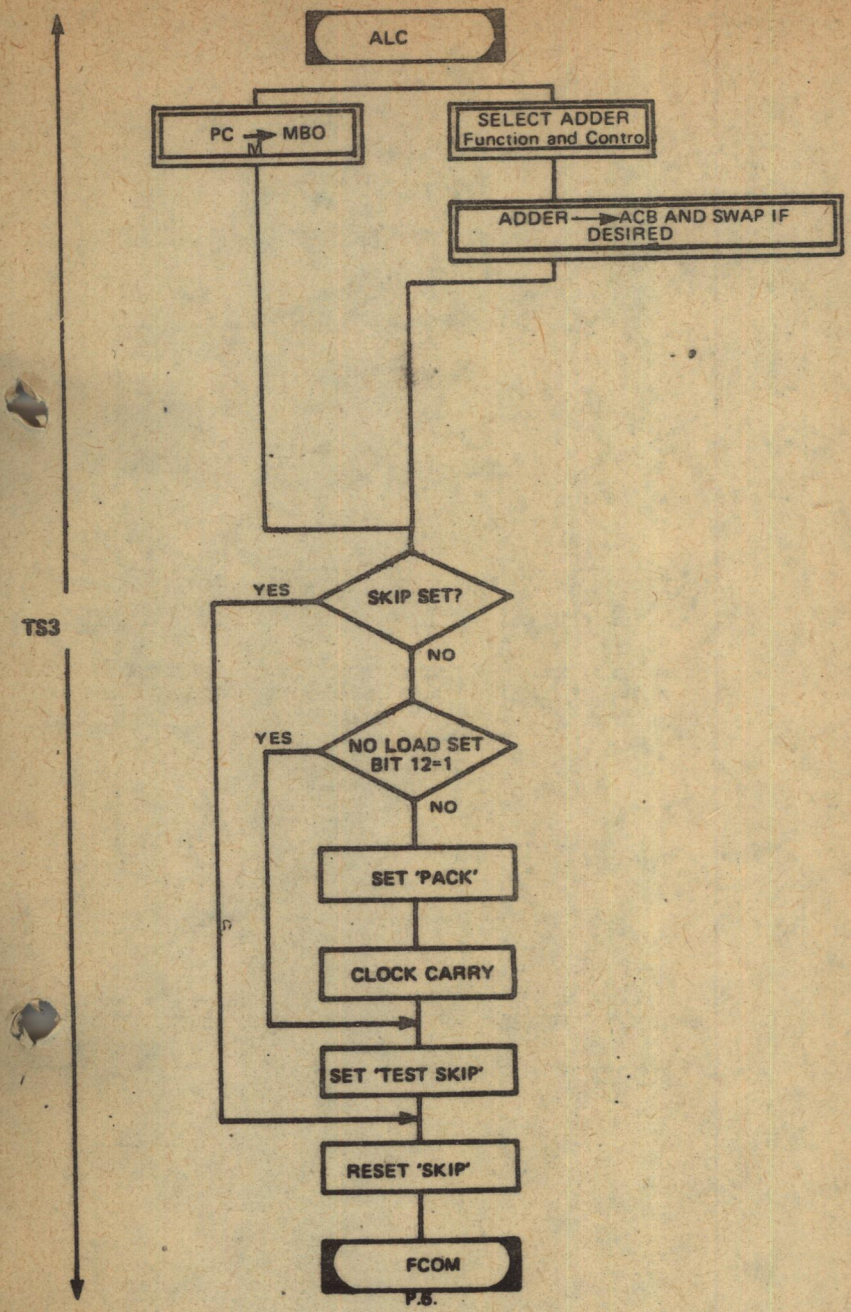


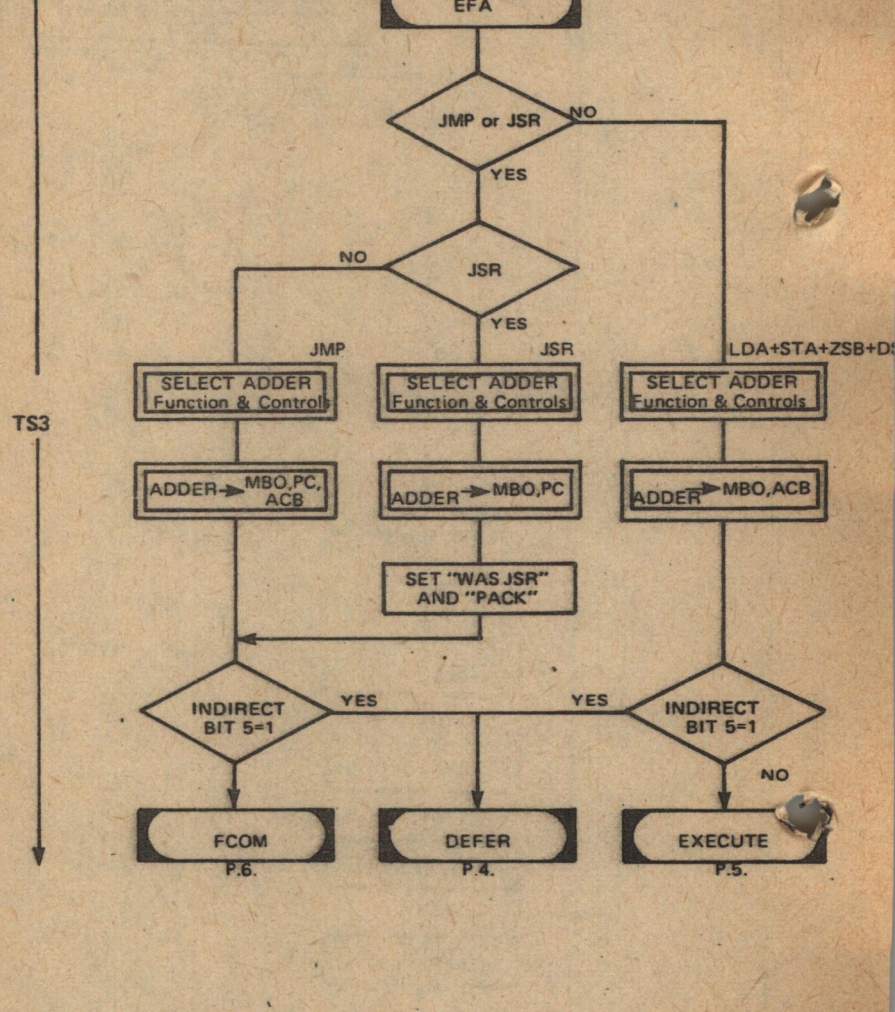
PARALLEL TRANSFER
OR SINGLE ACTION

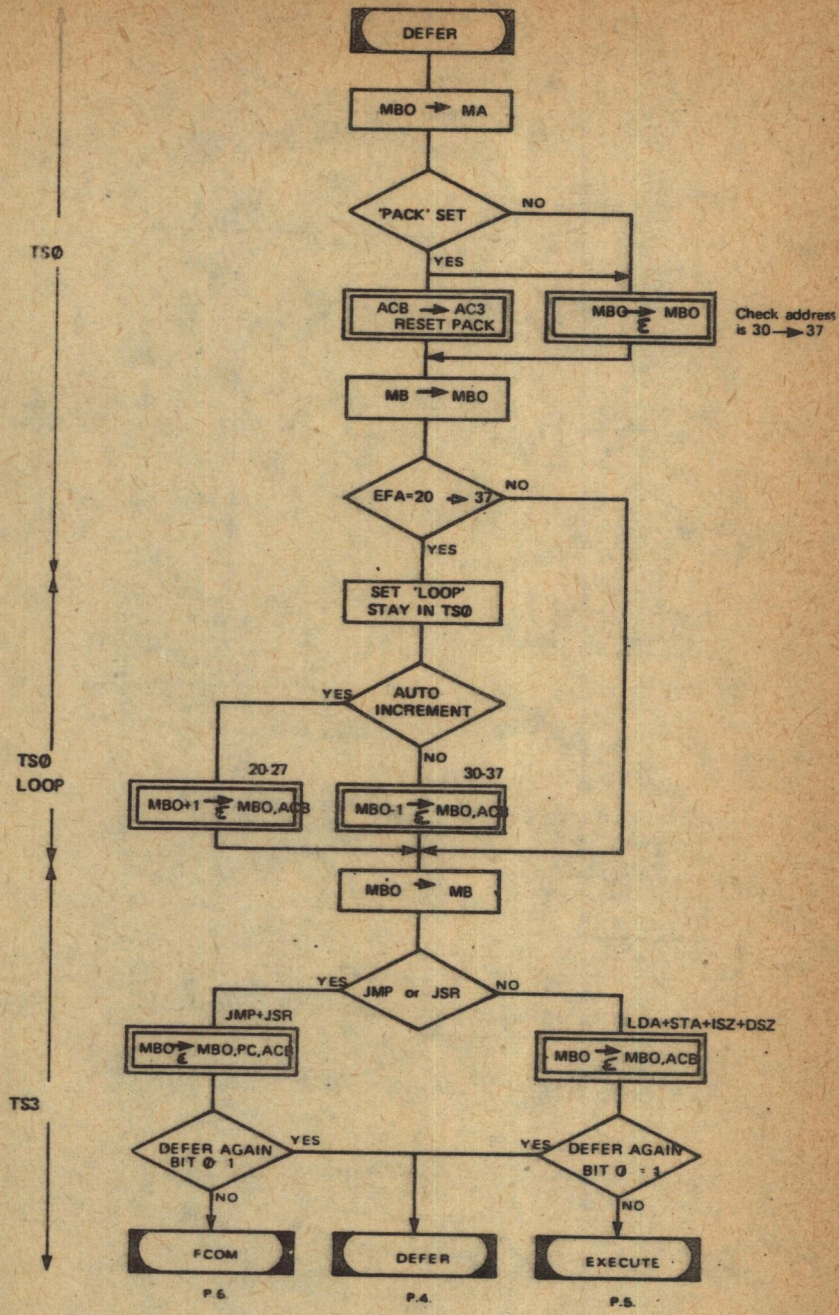
ACB —S→ AC
PC —M→ MBO
MBD+1 —ε→ MBO,PC

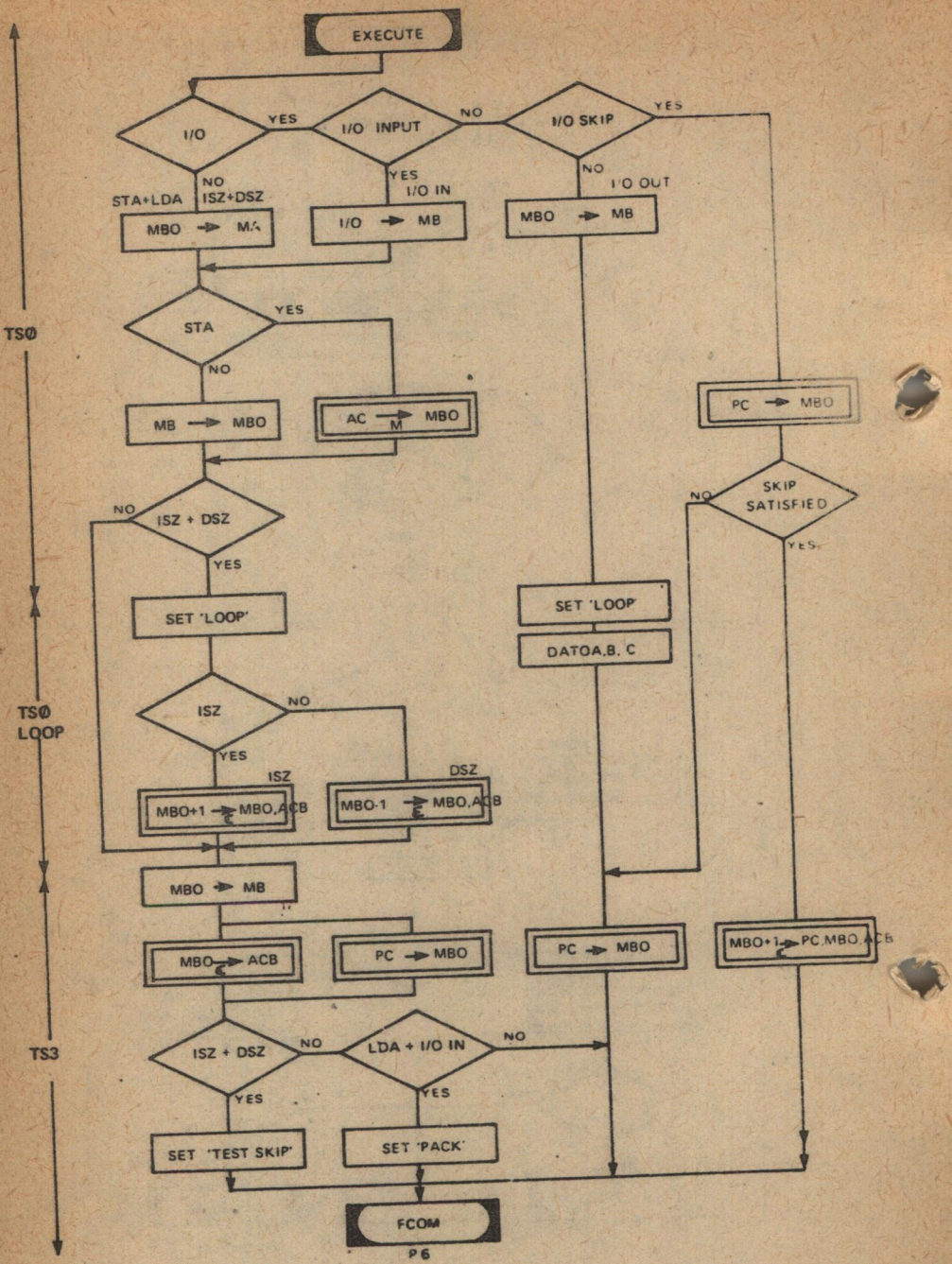
S = Through Shifter
M = Through Multiplexer
ε = Through Adder

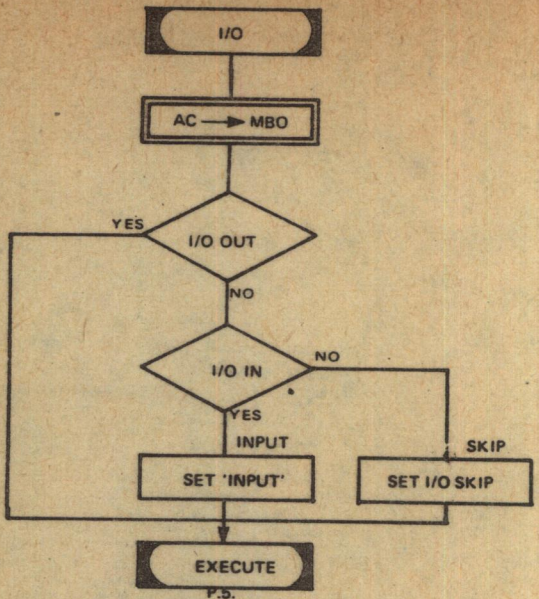

FETCH
MBO → MA
YES
PACK SET?
NO
ACB → AC
S
and shift if desired
MBO → MBO
M
MBO+1 → PC,ACB
RESET PACK
TEST SKIP SET?
YES
RESET TEST SKIP
NO
SKIP PENDING
YES
SET SKIP F/F
NO
MB → IR
& MBC
SKIP SET?
YES
NO
INSTRUCTION TYPE
EFA
P.3.
I/O
P.6.
ALC
P.2.
TSØ

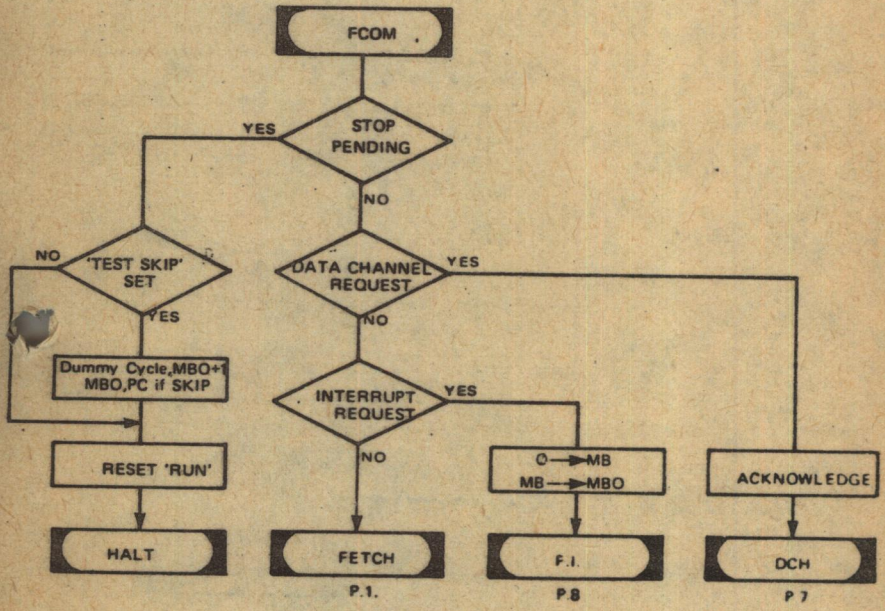

ALC
PC → MBO
M
SELECT ADDER
Function and Control
ADDER → ACB AND SWAP IF
DESIRED
TS3
YES
SKIP SET?
NO
YES
NO LOAD SET
BIT 12=1
NO
SET 'PACK'
CLOCK CARRY
SET 'TEST SKIP'
RESET 'SKIP'
FCOM
P.S.

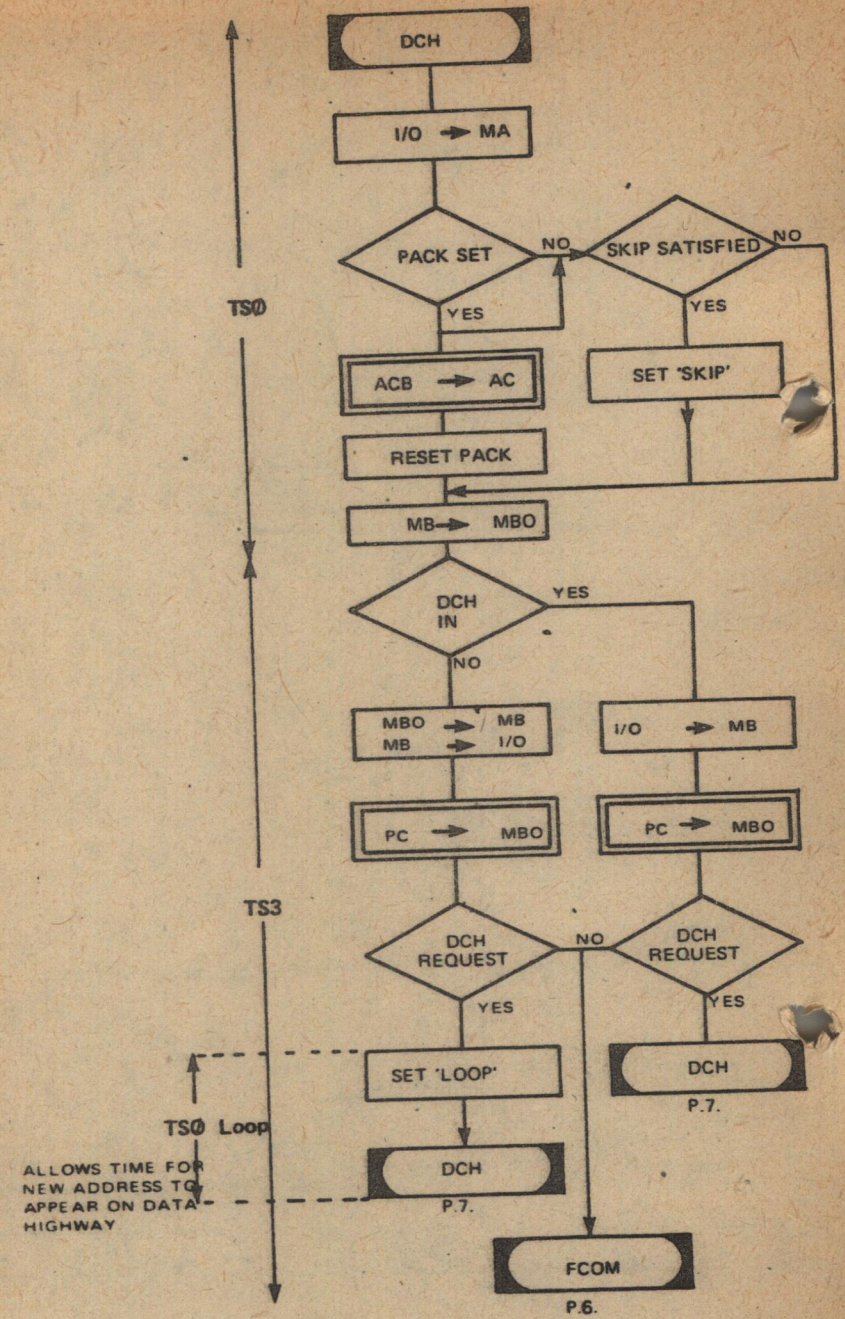

EFA
JMP or JSR
NO
YES
NO
JSR
YES
JMP
JSR
LDA+STA+ZSB+D
SELECT ADDER Function & Control
SELECT ADDER Function & Controls
SELECT ADDER Function & Controls
TS3
ADDER → MBO,PC, ACB
ADDER → MBO,PC
ADDER → MBO,ACB
SET "WAS JSR" AND "PACK"
INDIRECT BIT 5=1
YES
YES
INDIRECT BIT 5=1
NO
FCOM
P.6.
DEFER
P.4.
EXECUTE
P.5.

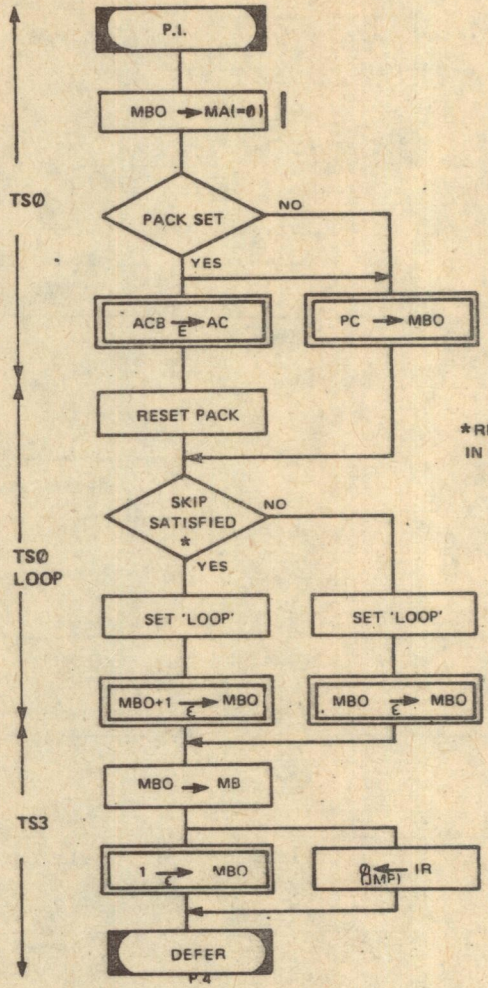

DEFER
MBO → MA
'PACK' SET
NO
YES
TSØ
ACB → AC3
RESET PACK
MBO → MBO
Check address is 30 → 37
MB → MBO
EFA=20 → 37
NO
YES
SET 'LOOP'
STAY IN TSØ
YES
AUTO INCREMENT
NO
TSØ LOOP
20-27
30-37
MBO+1 → MBO,AC3
MBO-1 → MBO,AC3
MBO → MB
YES
JMP or JSR
NO
JMP+JSR
LDA+STA+ISZ+DSZ
MBO → MBO,PC,AC3
MBO → MBO,ACB
TS3
DEFER AGAIN BIT Ø = 1
YES
YES
DEFER AGAIN BIT Ø = 1
NO
NO
FCOM
DEFER
EXECUTE
P.6
P.4
P.5

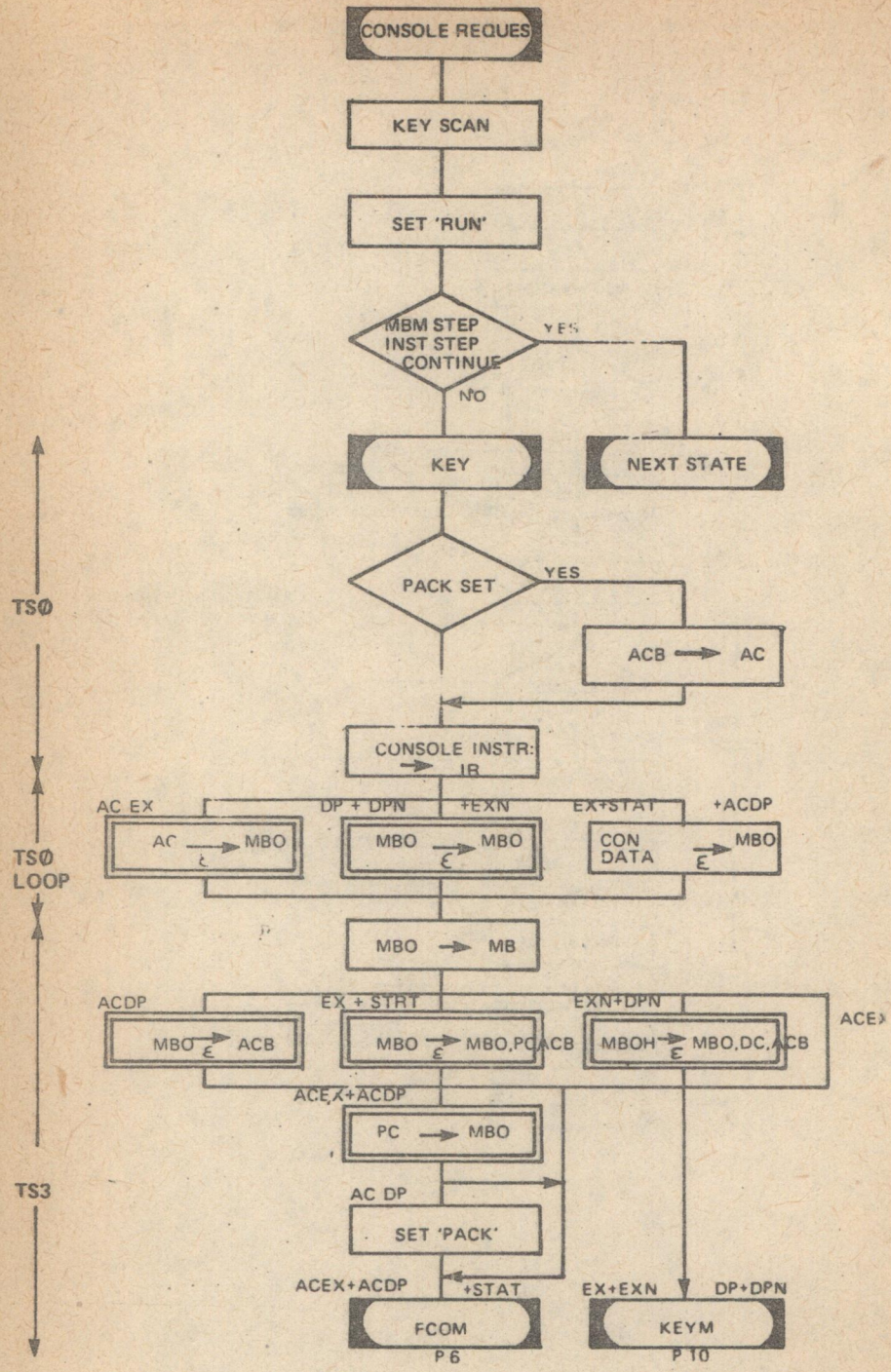

EXECUTE
I/O
YES
I/O INPUT
NO
I/O SKIP
YES
NO
STA+LDA
ISZ+DSZ
MBO → M
YES
I/O IN
I/O → MB
NO
I/O OUT
MBO → MB
TSØ
STA
YES
NO
MB → MBO
AC → M → MBO
PC → MBO
NO
ISZ + DSZ
YES
SKIP SATISFIED
NO
YES
SET 'LOOP'
SET 'LOOP'
DATOA,B, C
TSØ LOOP
ISZ
NO
YES
ISZ
MBO+1 → MBO,ACB
DSZ
MBO-1 → MBO,ACB
MBO → MB
MBO → ACB
PC → MBO
PC → MBO
MBO+1 → PC,MBO,ACB
TS3
ISZ + DSZ
NO
LDA + I/O IN
NO
YES
YES
SET 'TEST SKIP'
SET 'PACK'
FCOM
P6

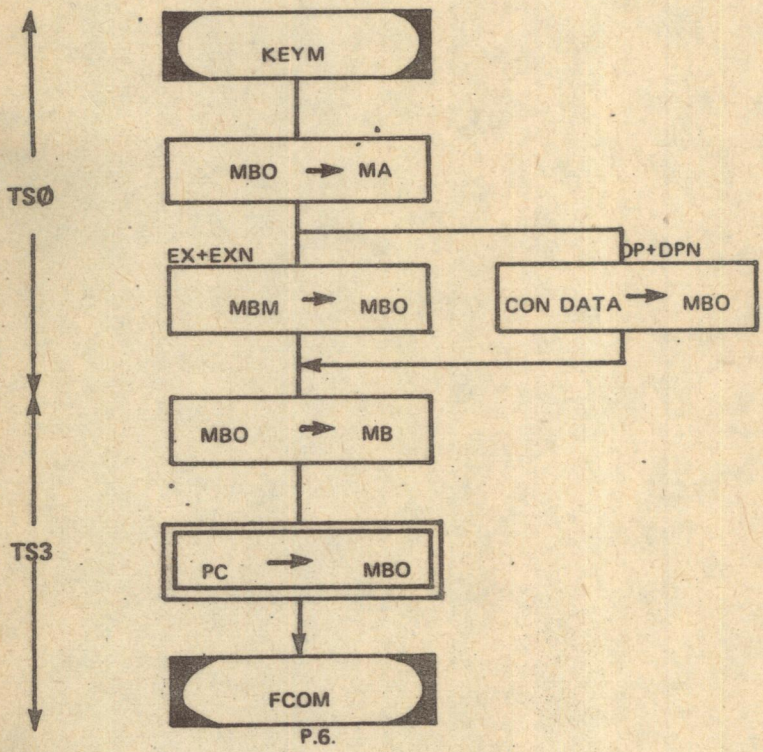

I/O
AC → MBO
YES
I/O OUT
NO
I/O IN
NO
YES
INPUT
SET 'INPUT'
SKIP
SET I/O SKIP
EXECUTE
P.5.


FCOM
YES
STOP PENDING
NO
NO
'TEST SKIP' SET
YES
DATA CHANNEL REQUEST
YES
NO
Dummy Cycle,MBO+1 MBO,PC if SKIP
INTERRUPT REQUEST
YES
RESET 'RUN'
NO
0 → MB
MB → MBO
ACKNOWLEDGE
HALT
FETCH
P.1.
F.I.
P.8
DCH
P.7


DCH
I/O → MA
PACK SET
NO
SKIP SATISFIED
NO
YES
YES
TSØ
ACB → AC
SET 'SKIP'
RESET PACK
MB → MBO
DCH IN
YES
NO
MBO → MB
MB → I/O
I/O → MB
PC → MBO
PC → MBO
TS3
DCH REQUEST
NO
DCH REQUEST
YES
YES
SET 'LOOP'
DCH
P.7.
TSØ Loop
ALLOWS TIME FOR NEW ADDRESS TO APPEAR ON DATA HIGHWAY
DCH
P.7.
FCOM
P.6.


P.I.
MBO → MA(=0)
TSØ
PACK SET
NO
YES
ACB → AC
PC → MBO
RESET PACK
*REFER TO SKIP DECISION IN FETCH FLOW DIAGRAM
SKIP SATISFIED *
NO
YES
TSØ LOOP
SET 'LOOP'
SET 'LOOP'
MBO+1 → MBO
MBO → MBO
MBO → MB
TS3
1 → MBO
Ø → IR
(JMP)
DEFER
P.4


CONSOLE REQUES
KEY SCAN
SET 'RUN'
MBM STEP
INST STEP
CONTINUE
YES
NO
KEY
NEXT STATE
PACK SET
YES
ACB → AC
CONSOLE INSTR: → IB
AC EX
DP + DPN
+EXN
EX+STAT
+ACDP
AC → MBO
MBO → MBO
CON DATA → MBO
MBO → MB
ACDP
EX + STRT
EXN+DPN
ACEX
MBO → ACB
MBO → MBO,PC,ACB
MBOH → MBO,DC,ACB
ACEX+ACDP
PC → MBO
AC DP
SET 'PACK'
ACEX+ACDP
+STAT
EX+EXN
DP+DPN
FCOM
P6
KEYM
P10
TSØ
TSØ LOOP
TS3


KEYM
MBO → MA
EX+EXN
DP+DPN
MBM → MBO
CON DATA → MBO
MBO → MB
PC → MBO
FCOM
TSØ
TS3
P.6.

8-K AND 16-K MEMORIES

SEECHECK CORE MEMORY

General Description

Seecheck employs either 8–K or 16–K memory boards to build up an overall size of up to 32–K of memory. Both types of boards are similar in mechanical construction, electronic circuits and principles of operation. A 16–K board has twice the core stack of 8–K board. The 16–K board may be considered as two halves each comprising 8–K memory.

These boards are installed in slots 2 through 12 of the 17 slot computer chassis. A memory board contains a 15–bit memory address register, a 16–bit buffer register, a core stack and associated sense/inhibit and line driver circuits. All memory addresses are considered contiguous in core with the first 3 bits of the memory address word (MSB 1, 2, 3) specifying the memory circuit board on which read/write operations will commence. Each memory board contains a decoder circuit which decodes the first three bits of the address word, enabling the selected memory board to be accessed. 8–K memories use bits 1 and 2 to determine the location in core the memory board is to reside (one of four 8–K areas) and bit 3 is used by the 8–K board itself to select the upper or lower (4–K) half of the board. Whereas in 16–K memory, bit 1 is used to determine which half of the total address field (32–K) the memory board is to be located (upper 16–K or lower 16–K). Bit 2 is used to select the upper or lower half of the 16–K board itself.

NOTE

The Seecheck system always performs a read/modify/write cycle regardless whether the information read from memory is to be modified or not.

Installation of Memory Boards

When installing a new memory board, the relevant pins on the jumper block (shown in Figs. 1A & 1B) must be checked for correct wiring links. These links are wired to enable the address decoder on the respective memory board to respond to a specific block of addresses (8–K or 16–K) in core since the memory address registers of all the boards are loaded with the same address at the same time.

8–K Memory Boards

Each 8–K memory plane is selected by the wire links as shown in Figure 1A. These links connect either the Ø or 1 side of the high order MA bits to an 'AND' gate. The output of this 'AND' gate will be true only if the code for which it is

wired is true and only then the memory can respond. This code is unique to that particular memory board. The jumper blocks are located on the component side of the board in the lower right hand corner. For convenience sake, it is usual to place the least significant 8—K board in the bottom of the four slots and the remaining three boards in the ascending order of significance. Before fitting the board it must be ensured that the wire links are correct for a selected address. Two or more identically addressed boards will give meaningless data on read back from memory. Addressing a non-existant location will return zero on read.

CAUTION:

NEVER PLUG IN A MEMORY BOARD WITH THE STACK FACING DOWNWARDS.

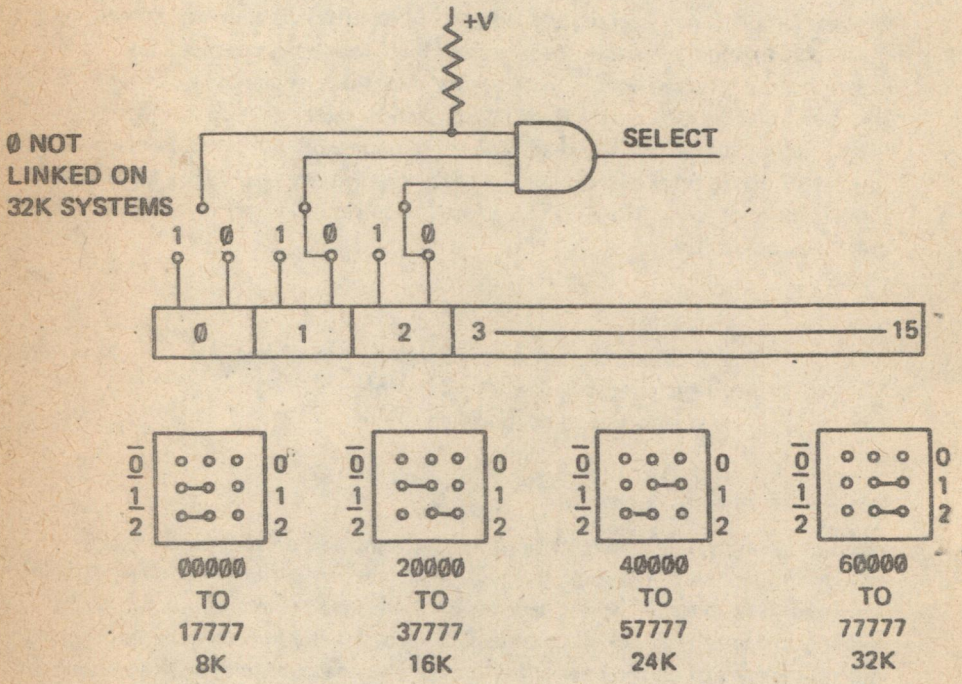


Figure 1A: 8K Board Select Wire Links

16–K Memory Boards

The jumper block for the DCC 16–K board is shown in Figure 4B and pin connections are tabulated as follows:

Location in Memory	Wire Links
1st 16–K Board	Pin 5 to 12
2nd 16–K Board	Pin 6 to 11

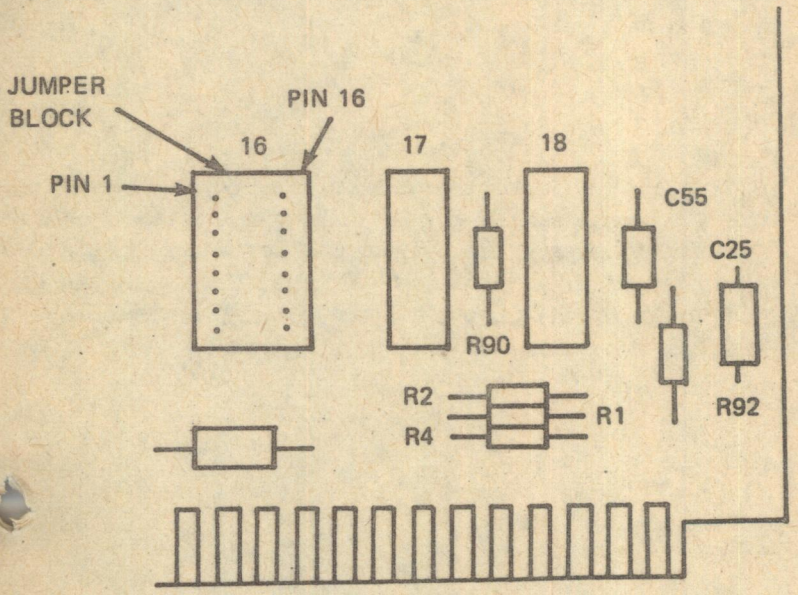


Figure 1B: 16K Board Select Jumper Block

When 8–K and 16–K boards are required to be intermixed to achieve a memory size up to 32–K, reference must be made to the memory board boundries shown in the following table:

Overall Memory Size	0	8–K	16–K	24–K	32–K
Memory Board Size	16–K		16–K		
	8–K	8–K	8–K	8–	

Note that 16–K board cannot be connected immediately following an 8–K single board.

Example:

A 16–K board is required to be added to an existing 8–K memory to achieve a 24–K capacity. Since a 16–K board can only be added to two 8–K boards, it is therefore suggested that the single 8–K be removed first. Then the 16–K board is connected for the lower 16–K position, i.e. pin positions 5 to 12 are jumpered on the 16–K board. The 8–K board is then added with its pin positions jumpered correctly as shown in Figure 4A.

Memory Before

1st

8 K

Memory After

1st	2nd	3rd
16–K		8–K

Review of Core Memories

A "BIT" of information can be stored in a ferrite core by magnetizing the core in one of two possible directions or "states", calling one state a "1" and the other state a "0" like a flip flop. Unlike a flip flop however, a core cannot be read simply by examining its output voltages.

A CORE IS READ BY FORCING IT INTO THE "0" STATE and then watching for the current pulse which is generated on a sense line when the core changes state.

If the pulse occurs, then the core must have been in the "1" state before it was switched. If no pulse occurs then the core must have already been in the "0" state because no transition took place.

Reading a core then always leaves it in the "0" state and although the information that it contained has probably been transferred to some other register, that information is no longer in the core and must be restored by a WRITE CYCLE if it is to be available again. Writing means setting the core to a one or a zero, depending on the state of a memory register that contains core-bound information.

Reading or Writing is a matter of sending current pulses along wires into the core; the direction of current relative to the core determines which state it will move into.

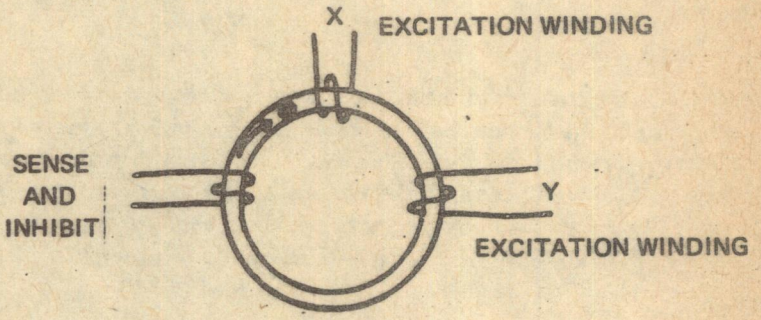


Figure 2: Simplified Schematic of a Memory Core

A core will remain in the "one" state until currents pass through the X & Y excitation winding and force it into the "zero" state. The transition causes a pulse to travel down the sense winding to detection logic.

(Transition implies induction)

The core can be reset to the "one" state by reversing the current in the X and the Y windings. The transition *will still cause a pulse* to be generated in the sense and inhibit winding, but the sense logic is disabled at this point.

The core memories we will be using contain many thousands of these ferrite cores strung together like beads on wires. Each core has three wires passing through it, and these wires carry the X and Y read and write currents and the pulses resulting from core transitions. The memories are wired so that the computer can select ANY GROUP OF 16 BITS AT ONCE and read or write a complete 16 bit word "IN PARALLEL".

A group of 16 cores is called an address and is selected by passing half the current required to switch the cores down the X and half down the Y winding. The windings are arranged such that the currents coincide at only one set of 16 cores. The combined effect of the current in these two wires is enough to flip those cores which were at a '1' to a zero. Each core that flips sends a pulse down its *OWN* third wire called a sense wire which is then fed into one flip flop of a 16 bit MEMORY BUFFER. The flip flop sets if it sees a pulse, and remains reset if there is no sense pulse. The register which selects the X & Y wires or lines is called the ADDRESS Register.

Write Cycle

Restoring the contents of the address involves resetting those core bits that set ones into the Memory buffer. This is done by sending currents in a reverse direction through the X and Y lines which coincide at that address and at the same time INHIBIT currents to those bits which should remain in the "0" state. The contents of the memory buffer could be changed before this write cycle so that new information can be entered into this address.

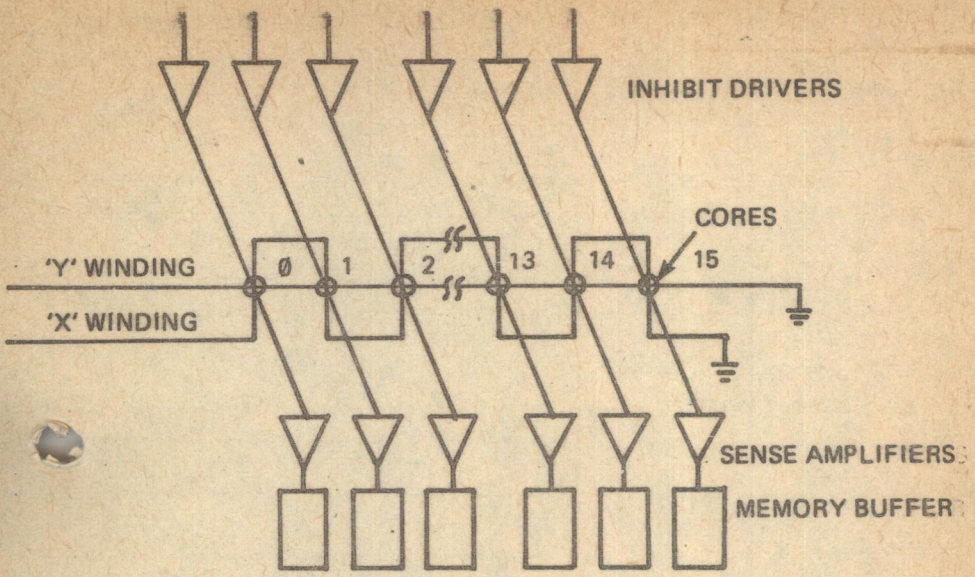


Figure 3: Coincident current address selection

To select the above location (Fig.3), the address specified is fed through decoding logic to select the appropriate X & Y windings, half the current needed to switch the core is sent down the "Y" wire and half down the "X" wire. Where the two currents meet, that core is energised. The arrangement shown (Fig.3) is such that 16, and only 16 bits (cores) are selected at once, thus a 16 Bit word can be selected by giving a specific number (address) to the X & Y decoders.

The memories used on the basic computer consist of cores arranged in a three wire 3D scheme in which the sense and inhibit functions share the same wire.

The cores are laid out in a single plane, and wired together in a "bowtie" pattern shown in Fig. 4. Each 8—K plane is assembled on a "Daughter board" which is mounted on a 15" x 15" "Mother" board where most of the memory logic is located. Power is supplied from the B.C.G. power supplies.

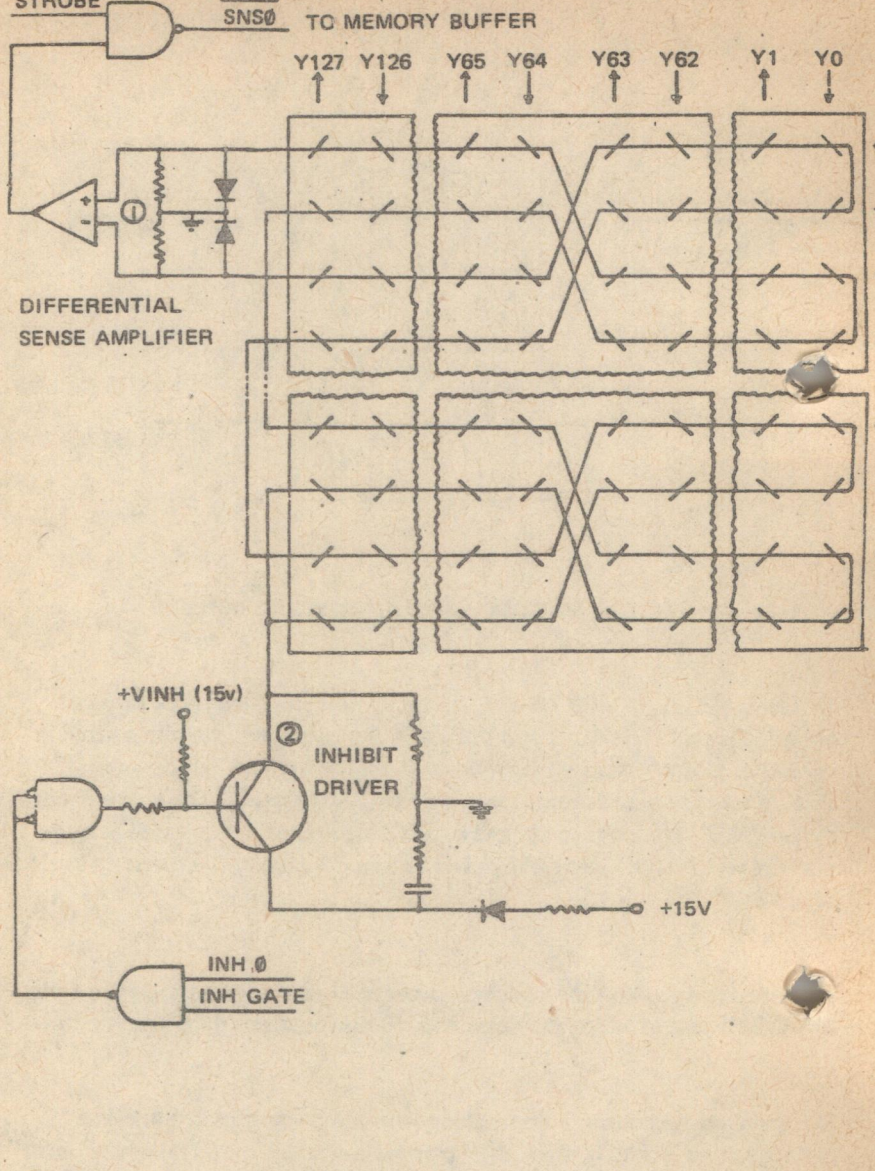


Figure 4: Simplified Schematic of the Core Memory Sense & Inhibit Line

Sense and Inhibit (refer to Fig. 3)

The sense and inhibit functions share the same wire. The sense circuitry (1), sees both ends of the wire and detects core turn-over pulses with a differential amplifier. The output of this amplifier is examined at STROBE TIME.

The inhibit logic (2) drives + 15 VDC level into the middle of the same wire at INHIBIT time. The current is divided and passes through all cores to ground through the diodes at the other end. Note that the inhibit current for any particular bit passes through the core for that bit in all addresses. Where the X & Y currents are coincident (i.e. at the address in which the data is to be stored) if the inhibit current is present half of the X & Y current is cancelled out and the core will remain in the zero state. If the inhibit current is not present a 1 will be written into that core. At all other addresses (i e. where X & Y are not coincident) the inhibit current is not sufficient to disturb the core.

Data Transfer

Each 8 K memory contains drivers, sense amplifiers, a memory address register, a memory buffer, multiplexor, memory select logic, and I/O Drivers. (see Fig.5).

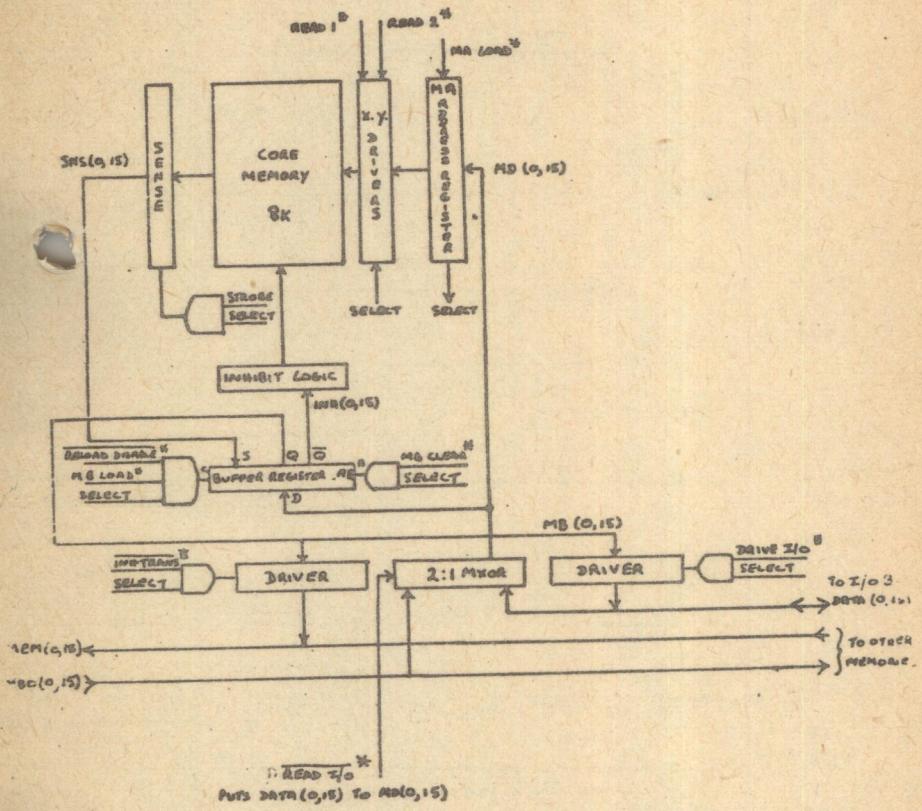
Data is transferred between memory and the CPU and I/O device along three data buses called:–

MEM which transfers data from memory to the CPU.

MBO which transfers data from the CPU to the memory.

DATA which transfers data between memory and I/O devices in either direction.

During a typical FETCH instruction the CPU outputs the memory address on the MBO 0–15 data lines and then issues MA LOAD. READ I/O is high, so the address is strobed into the memory address register and is output to the driver select logic. Then, READ 1 and READ 2 are issued gating the X & Y currents to the selected address. A little later STROBE is outputted by the CPU which gates all core pulses into their corresponding memory buffer bits. The memory buffer is then re-read back into core by reversing all the driver currents and gating the INHIBIT signal issued by the CPU to those bits which are not to be set to one. If the contents of the address is to change, the memory buffer is loaded with the new word before the address is re-written, i.e. before INHIBIT is issued.



* ISSUED BY CPU.

Figure 5: System Block Diagram

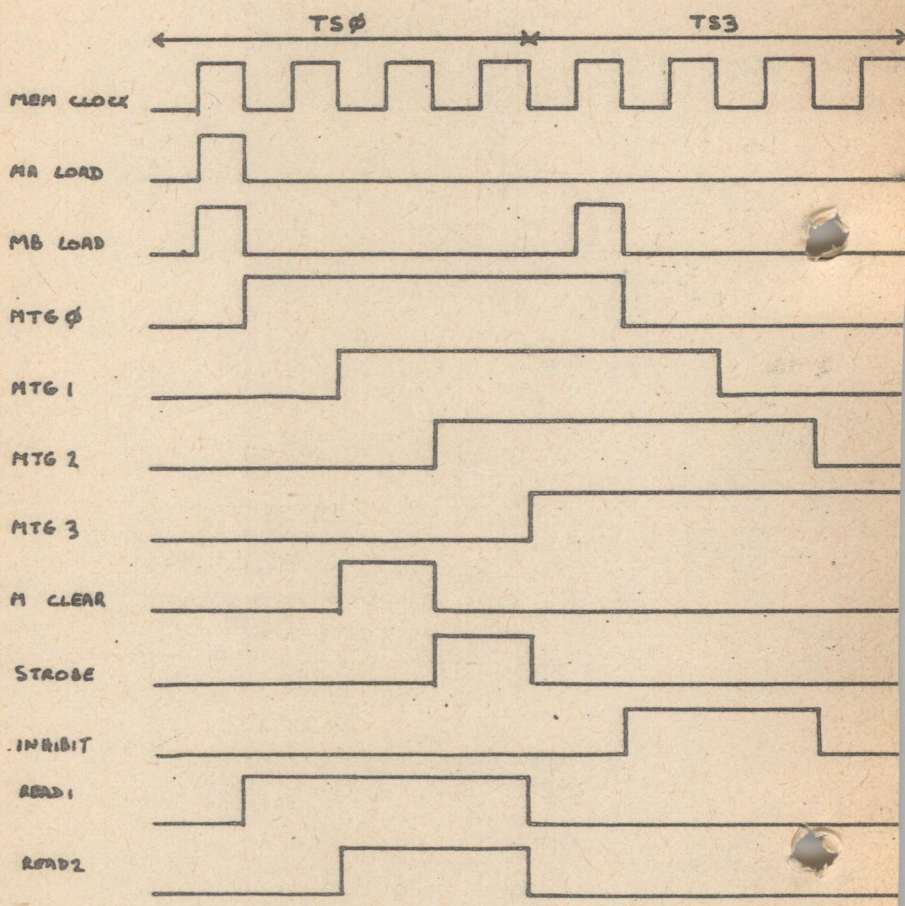


Figure 6: 8 K Memory Timing

LOGIC DESCRIPTION: Logic Prints 8 K. 00127. 5 sheets

INHIBIT LOGIC: Sheets 1 and 2

Example description of Bit Ø. The inhibit logic comprises:—

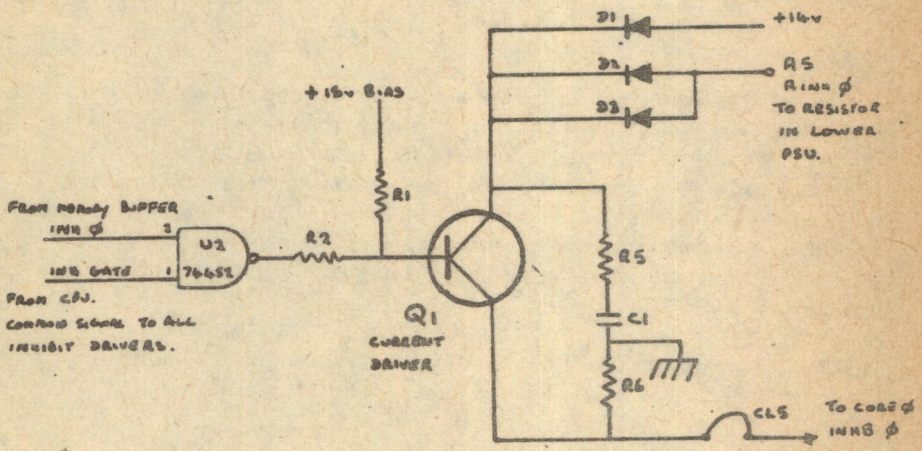
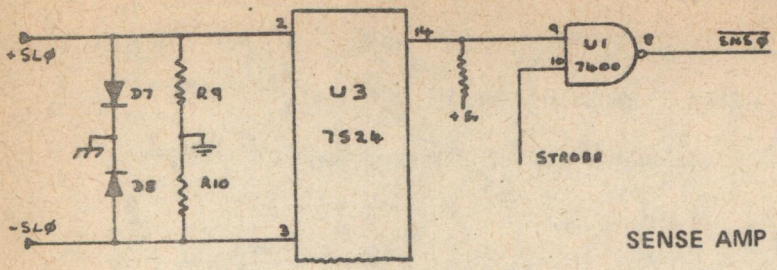


Figure 7

Suppose we wished to write a data pattern into a core location, i.e. all Bits to be "one" except bit zero. The data from the CPU passes through the multiplexer (Sheet 3) to the memory Buffer D FLOPS, all of which are set at MB LOAD time excepting for Bit Ø, i.e. the Q side will not change because its input is Ø. We can see that **INHØ will be true** and **INH1 — INH15 will be false.** At WRITE MEM time current is applied to all 16 cores at the address we have specified and will attempt to write all ones in all 16 Bits. However signal, INHIBIT GATE, from the CPU is already true at pin 1 of U2, this is "anded" with INHØ from the memory buffer, with the result that, current transistor Q1 is switched on, sending current down Bit Ø inhibit winding and cancelling out the effect of the X & Y current trying to force it to one state.

Sense Logic Sheets 1 and 2

The direct set inputs of the memory buffer $\overline{\text{SNS0}}$ — $\overline{\text{SNS15}}$ (Sheet 3) come from each of the sense amplifiers.

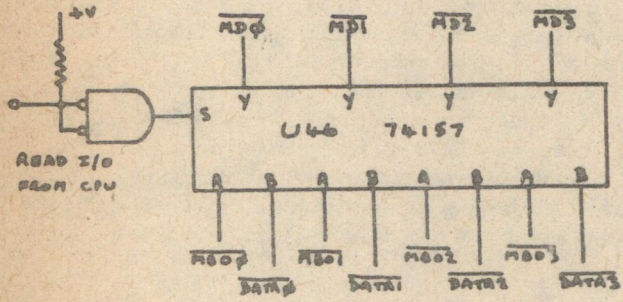


SENSE AMP BIT ZERO

+SLØ and SLØ are the two ends of the sense line running through bit zero core. Each time that a core which is in a 1 state is read a pulse is induced onto the sense winding for that bit. A core already in the zero state does not produce a detectable pulse. The X & Y currents change the one bit to a zero, the induction caused by this change of magnetic state, is picked up by the sense windings which feed into a differential amplifier U3 to appear at its output (Pin 14), this output is then strobed into the *memory buffer* with the common gating signal STROBE.

NOTE: a differential probe is required if the waveforms on the inputs to the sense amplifier are to be displayed on an oscilloscope.

U46–U40–U34–U28 comprise a two input 16 Bit multiplexor consisting of 16 FLIP FLOPS, INPUTS $\overline{\text{MBOØ}}$ – $\overline{\text{MB015}}$ are the data and address lines from the C.P.U. Inputs $\overline{\text{DATAØ}}$ – $\overline{\text{DATA15}}$ are the data lines from the I/O devices.



TRUTH TABLE

S	A	B	Y
Ø	1	X	1
Ø	Ø	X	Ø
1	X	1	1
1	X	Ø	Ø

X = DON'T CARE

Normally READ I/O is high and input A from MBO is gated straight through to output Y. During I/O, READ I/O goes low and disables MBO path through the multiplexer allowing $\overline{\text{DATA}}$ through to output Y.

Memory Buffer MBØ – MB15

The output of the multiplexer goes to the MEMORY ADDRESS register and the MEMORY BUFFER.

$\overline{\text{MB CLEAR}}$ is used to reset all 16 bits of the memory buffer.

The clock used to gate the input signals into the Memory buffer is an "AND" of MB LOAD and SELECT. The $\overline{Q}$ side of each F/F $\overline{\text{INHØ}}$ – $\overline{\text{INH15}}$ goes to each inhibit driver. The Q side drives two sets of NAND gates. MEMØ – MEM15 are the memory bus drivers, the outputs of which go to the C.P.U. The common gating signal is a function of $\overline{\text{INH TRANSFER}}$ and SELECT.

$\overline{\text{DATAØ}}$ – $\overline{\text{DATA15}}$ are the I/O OUT BUS DRIVERS whose outputs go to peripheral equipment, the common gating signal is a function of $\overline{\text{DRIVE IØ}}$ and SELECT.

Input – Output Sheet 3

During an output I/O instruction (DOA, DOB, DOC), data moves from the source AC into the M.B.O. and onto the MBO Bus. From the bus it is strobed into the memory MB register through the multiplexer with SELECT and MBLOAD. INH TRANSFER is low thus inhibiting $\overline{\text{MEMØ}}$ – $\overline{\text{MEM15}}$. $\overline{\text{DRIVE I/O}}$ is low thus enabling the data through the I/O bus drivers to the peripheral device on $\overline{\text{DATAØ}}$ – $\overline{\text{DATA15}}$.

READ 1 & READ 2 are not generated so the data is not strobed into memory.

During an INPUT I/O instruction (DIA, DIB, DIC), the peripheral device inputs to the CPU. $\overline{\text{READ I/O}}$ goes low and switches the data through the multiplexer to the MB which is clocked in by SELECT & MB LOAD. $\overline{\text{DRIVE IO}}$ goes high and inhibits $\overline{\text{DATAØ}}$ – $\overline{\text{DATA 15}}$. $\overline{\text{INHIBIT TRANSFER}}$ & SELECT gates the data through the MEM BUS drivers to the MEM BUS, and READ 1 and READ 2 are not generated. From the MEM BUS the data is strobed into the MBO which moves through the adder to the ACB and into the A.C.

Memory Control Signals Sheet 5

All inputed signals and associated driver gates can be found on Sheet 5, all have been described apart from XRS, XYS, YWS, which are the supply currents for the X & Y drivers and are derived from V mem from the P.S.U. CL1 – CL4 are the current test-point loops where the current waveforms can be monitored with a current probe (see Fig. 10).

The Memory Address Register Sheet 5

This consists of 16 Flip Flop U47–U41–U35 and U29. Addresses from the mem bus MDØ – MD15 are applied tn the inputs and clocked with MALOAD. The output gives MAØ – MA15 (note outputs Ø ,1, and 2 enable select only if the jumper block is correctly set up). Although MAØ – MA15 are shown they are not used, MAØ – MA15 are fed through inverting drivers to give BMA 3 – BM15 and MA3 – BMA15. MA1 – MA2 are used to select the particular 8K block within the current maximum capacity of 32K. MAØ would be used if at any time the maximum amount of core available was extended to 64K.

The Addressing System Sheet 15

To address 8K of core a 13 bit address is required (8K Decimal = 20000 OCTAL = 13 Bits). The 13 bits are split between the X and Y lines; the least significant six bits (10 through 15) are decoded to select the appropriate X winding, and the most significant seven bits (3 through 9) are decoded to select the appropriate Y winding. The X and Y decoding is handled completely separately, the only major difference between the two being that the Y decoding logic has to handle a 7 bit address and the X a six bit address. To all intents and purposes they work in the same way as each other and therefore only the X decoding will be explained in detail.

Consider a WRITE at address Ø: BMA1Ø to BMA15 are all true. Referring to the logical representation of the 75324 Fig. 8 it will be seen that in this case U82 and U83 are inhibited by BMA1Ø being false (pin 5), and that U84 is inhibited by BMA11 being false (pin 4). On U85, BMA1Ø. BMA11. BMA12. WRITE MEM turns on the gate driving pin 10 (X source). On U75. BMA15. BMA14. BMA15. WRITE MEM will cause the gate driving pin 14 to turn on (X sink). Thus a current path through the X winding is established via the source at pin 10, U85 and the sink at pin 14, U75. (See Fig. 9).

If we now consider a READ cycle at address 0: the BMA lines 10–15 remain in the same state but for a read cycle instead of WRITE MEM, READ 1B, is true. Referring to Fig. 8 it may be seen that on U85 instead of pin 10 being active, pin 9 (X sink) is turned on. On U75 instead of pin 14 being active, pin 12 (X source) is turned on. Thus a current path in the reverse direction to that for a WRITE Cycle is established through U75 pin 12 (X source) and U85 pin 9 (X sink). (See Fig. 9).

Thus for any particular address an X winding is selected and the correct current path direction chosen depending upon whether the cycle is READ or WRITE.

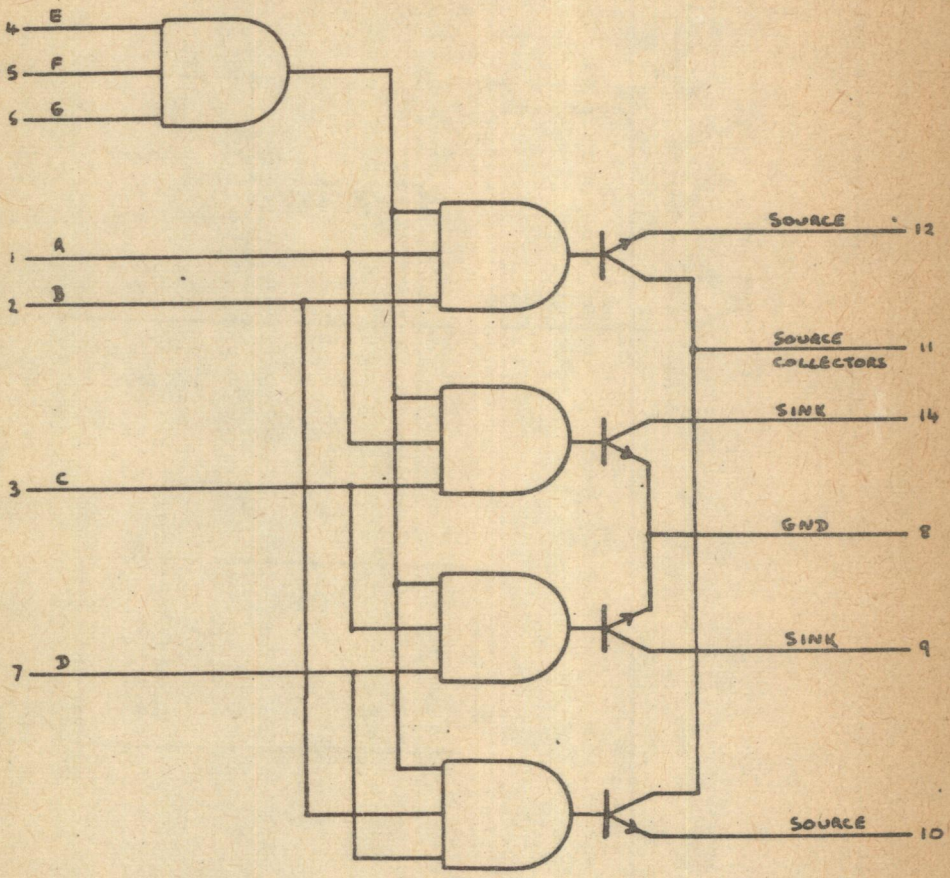


Figure 8: SN 75304

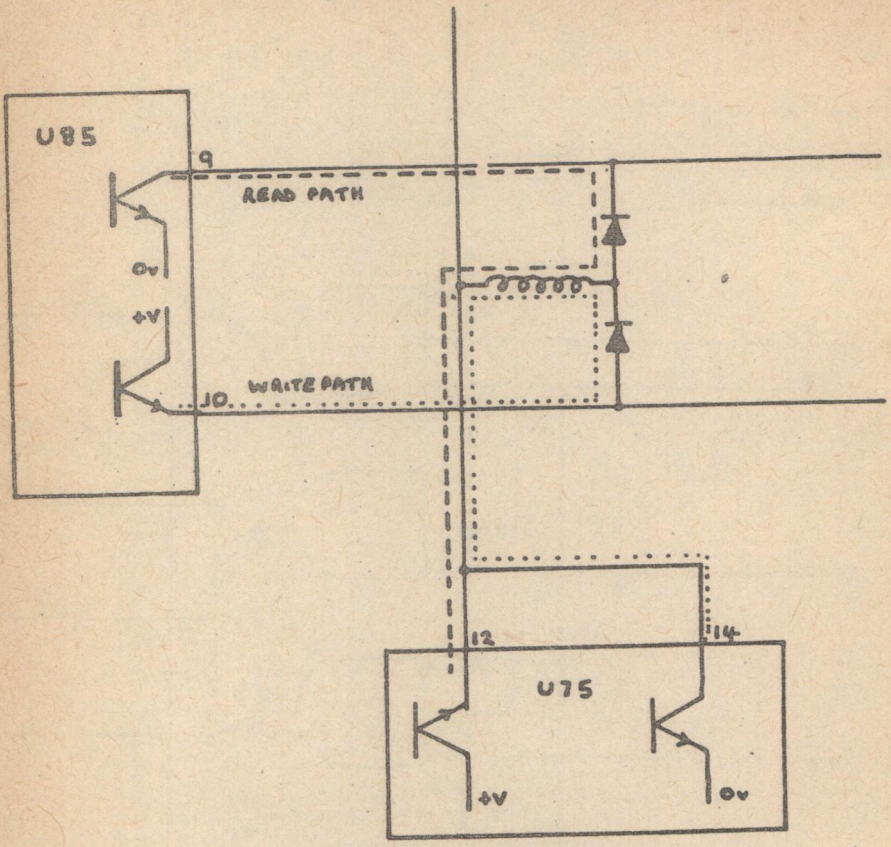


Figure 9: Read & Write Paths

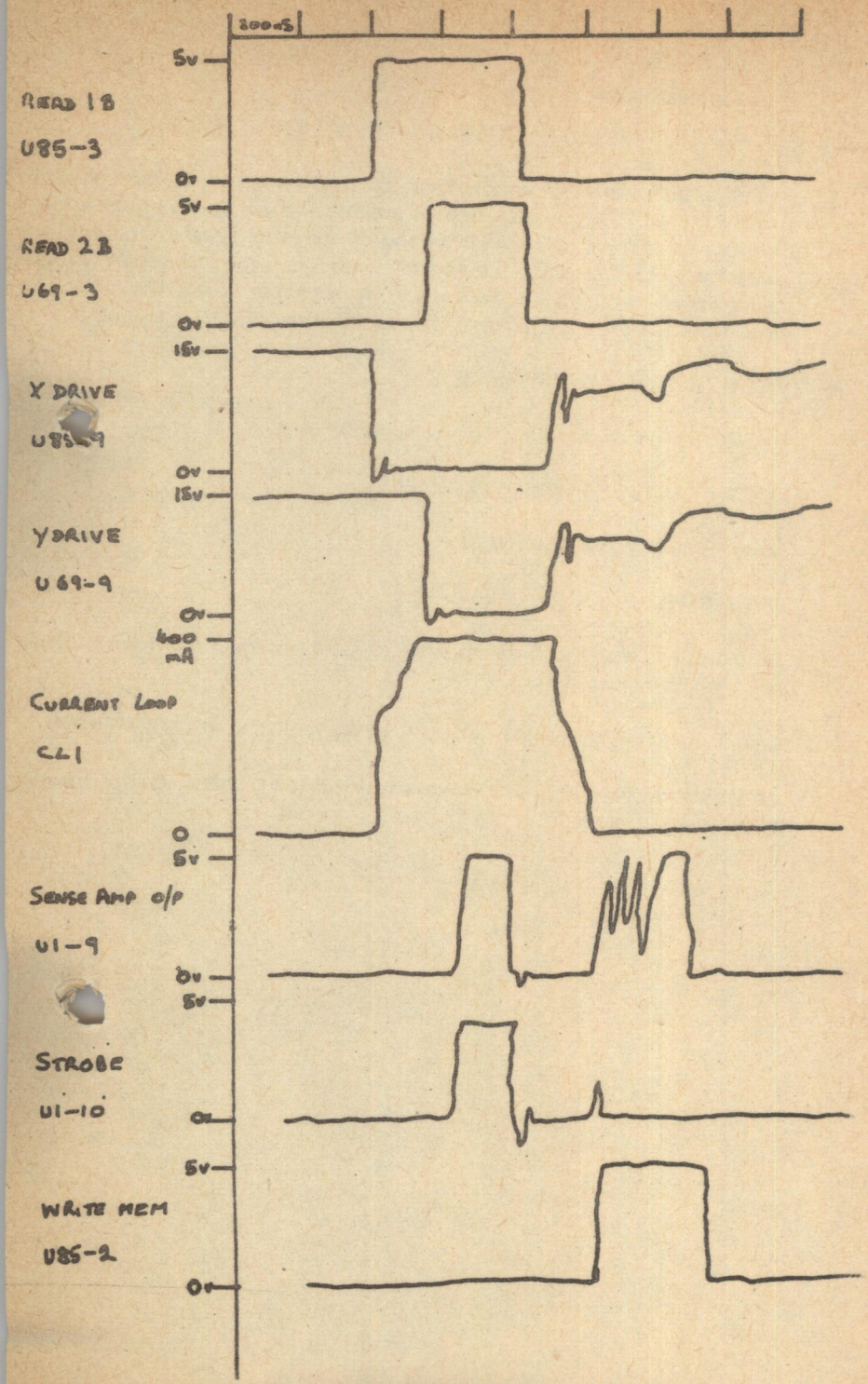


Figure 10: Memory Timing Diagram

Some Typical Faults

SEVERAL DIFFERENT LOCATIONS "PICK" THE SAME BIT.

This is an indication that although we specified zero for that particular bit a one was read. The inhibit amplifier logic should be looked at, could be that it is not turning on for that bit and on the write cycle the bit will always be a one. Common fault on 8K memorys is the solder joints from inhibit driver output to the stack itself. It might have a good output signal from the amp. but it never reaches the stack due to a dry joint.

VMEM OUT OF ADJUSTMENT.

EXERCISOR fails every hour or so, adjust VMEM.

DOESN'T MAKE SENSE TYPE FAULTS.

Noise. Ensure that a shield is fitted.

DROP BITS.

An indication that the sense amplifier is not detecting a transition. Check sense amplifier bits effected.

CAN'T READ AND WRITE AT ALL INTO A BANK OF LOCATIONS.

An indication that you have an address driver fault, check address drivers of locations effected.

MEMORY TEST PROGRAM

00	024437	START	LDA 1, PATAD	AC1 = Address of pattern store
01	030441		LDA 2, STRTB	AC2 = BUFF STRT
02	034441		LDA 3, ENDB	AC3 = MEM END
03	020136		LDA 0, ATNXT	AC0 = AC 2 + 1
04	041000	LOOP 1	STA 0,0,2	PUT ADDRESS = @ ADDRESS+1
05	101400		INC 0, 0	
06	151400		INC 2, 2,	
07	172414		SUB≠3,2,SZR	END OF MEMORY
10	000774		JMP LOOP 1	NO
11	045000		STA 1,0,2	YES: PUT LAST LOCATION = PATTERN ADDRESS
12	030430	AGAIN	LDA 2,STRTB	AC2 = BUFF STRT
13	024423		LDA 1,BIT 0	AC1 = 077777
14	020424		LDA 0,PATRN	AC0 = PATTERN
15	100000		COM 0, 0	COMPLEMENT PATTERN
16	123400		AND 1, 0	REMOVE BIT 0
17	043000		STA 0 @ 0, 2	LONG INDIRECT ENDS AT LAST LOCATION NEW PATTERN NOW IN 'PATRN'
20	027000		LDA 1 @ 0, 2	LONG INDIRECT ENDS AT LAST LOCATION ACTUAL LOAD SHOULD HAVE BEEN FROM 'PATRN'
21	106414		SUB ≠ 0, 1,SZR	AC0 = AC1
22	063077		HALT	NO
23	020416		LDA 0,ATNXT	AC0 = @ BUF STRT+1
24	025000	LOOP2	LDA 1, 0, 2	AC1 = BUF DATA
25	106414		SUB ≠ 0, 1,SZR	AC0 = AC1
26	004406		JSR NHALT	NO
27	101400		INC 0, 0	YES
30	151400		INC 2, 2	
31	156414		SUB ≠ 2, 3, SZR	END OF MEMORY
32	000772		JMP LOOP 2	NO
33	000757		JMP AGAIN	YES ROUND AGAIN
34	063077	EHALT	HALT	AC0 = CORRECT DATA
35	000743		JMP START	AC2 = INCORRECT DATA
36	077777	NBIT0	077777	
37	000040	PATAD	PATRN	*
40	025252	PATRN	025252	
41	100045	ATNXT	@ BUF + 1	*
42	000044	STRTB	BUF	*
43	017777	ENDB	017777	LAST ADDRESS TO BE TESTED
		BUF		

The program can be relocated at any address, but the Locations * must be changed by the relocation amount.

DEPOSIT PROGRAM

This will deposit the contents of AC0 in the address selected on the switches. The switches may be changed whilst the program is running. Useful for checking address faults whilst scoping the memory.

```
00   063077        HALT
01   070477        READS, 2          AC2 = ADDRESS
02   060200        NIOC              CLEAR CAN BE USED AS
                                         SYNC (A50)
03   041000        STA 0, 2
04   000775        JMP . -3
```

CLEAR CODE

```
00   042020        STA 0 @ 20
01   000000        JMP . -1
20   000020
```

STORE ADDRESS IN ADDRESS

```
00   055400        STA 3, 0, 3
01   175104        INC 3,3,SZR
02   000000        JMP 0
03   063077        HALT

                   AC3 = 00004
```

To make this store any data pattern in core put

```
00   041400        STA 0, 0, 3
                   PUT AC0 = DATA PATTERN
```

DISC CONTROLLER

DISC CONTROLLER DESCRIPTION

The controller is set up by issuing a DOA, DOB, DOC and a start pulse from the NOVA.

DOA

This loads the operation register, Mode register and drive register.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
			OP		MODE							DRIVE			
READ			0	0	0	0						24 Sector	0	0	0
WRITE			0	1	0	1						12 Sector	1	0	1
CHECK			1	0	1	0						36 Sector	2	1	0
RESET			1	1	1	1						Invalid	3	1	1

OP Register

If read is selected the record is read from the disc into memory. If write is selected the record is written from memory into disc. If check is selected the record is read but is not transferred to memory. This is used to check for a correct write as a checksum error will still occur for any error.

If reset is selected, the heads of the selected drive are restored to zero.

Mode register

This selects either 24, 12 or 36 sector mode. This also decides the number of words to be transferred i.e. 200_8, 400_8 or 100_8.

Drive register

Normally drive 0 is selected but it is possible to 'daisy chain' more drives into the system. If this is done then the drive itself must be addressed correctly by changing jumpers inside the unit.

DOB

This loads a register with the starting address of the data block in memory. The register is incremented by one after each transfer.

Bits 1–15 of the DOB are used and constitute an address in the range 0 - 32K

This loads a block register with the required track and sector. The upper or lower head is also selected.

Ø	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Cylinder/Track Ø – 2Ø2 Physical Sector Pseudo

1Ø

Ø – 312_8 Ø – 11_{10} Ø – 13_8 Sector

HEAD

Ø – LOWER

In 24 sector mode the Pseudo sector will be Ø or 1, in 12 sector mode it w[illegible] be Ø, and in 36 sector mode Ø or 2.

Write

When the DOA loads the Drive, Mode and OP registers the new values of Drive number and mode are compared. If they do not compare then the disc changing F/F is set and is not reset until the index mark is received.

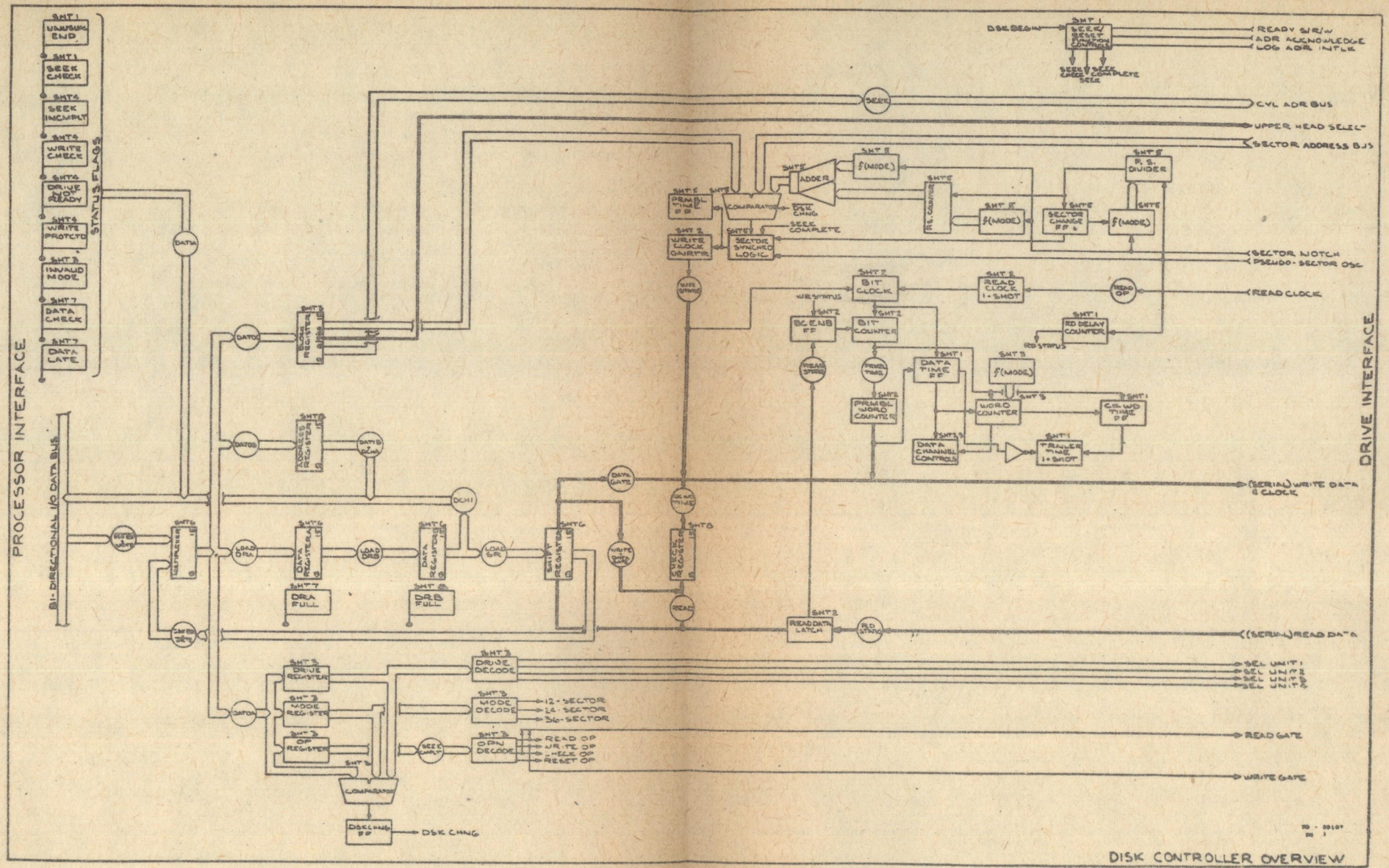
As soon as the start pulse is received Disc Begin is generated which sets the Seek F/F. The track address is sent to the drive together with Address Strobe. Address Acknowledged e is received from the drive as soon as it has completed the difference calculator, this resets address strobe. When the drive has got to the correct track it sends a Ready signal back which resets the Seek F/F. This allows the write operation to start.

The correct sector is found by comparing the number in the block register with the sector address from the drive and the pseudo sector calculated in the controller. When a sector notch occurs the Pseudo Sector Divider (8 bits) and Counter (4 bits) are preset to the complement of the required count (140_8, 260_8, 313_8 and 17_8, 16_8, 15_8 for 12, 24 and 36 sector mode respective[illegible] Taking 24 sector mode, this is calculated from:–

Time for 1 sector in 12 sector mode – $\dfrac{10^6 \times 60 \text{ us}}{1500\text{rpm} \times 12}$ = 3333u Sec

To allow for mechanical variations this is taken as 3200 uS
So for 24 sector mode each pseudo sector = 1600 uS
The pseudo sector oscillator is 50KHZ (20 uS rate)
We need therefore to count 80 pulses for each pseudo sector

$80_{10} = 120_8$ and two's complement of this is 260_8


PROCESSOR INTERFACE
DRIVE INTERFACE
STATUS FLAGS
UNUSUAL END
SEEK CHECK
SEEK INCMPLT
WRITE CHECK
DRIVE NOT READY
WRITE PROTCTD
INVALID MODE
DATA CHECK
DATA LATE
BI-DIRECTIONAL I/O DATA BUS
DATA
DATOC
DATOB
DATOA
LOAD DRA
LOAD DRB
LOAD SR
DRA FULL
DRB FULL
DCHI
DATA GATE
READ
READ DATA LATCH
RD STATUS
DRIVE REGISTER
MODE REGISTER
OP REGISTER
DRIVE DECODE
MODE DECODE
OPN DECODE
12-SECTOR
24-SECTOR
36-SECTOR
READ OP
WRITE OP
CHECK OP
RESET OP
COMPARATOR
DSKCHNG FF
DSK CHNG
SEEK
ADDER
f(MODE)
P.S. DIVIDER
SECTOR CHANGE FF
SECTOR SYNCHRO LOGIC
SEEK COMPLETE
BIT CLOCK
READ CLOCK 1-SHOT
READ OP
BC ENB FF
BIT COUNTER
RD DELAY COUNTER
DATA TIME FF
PRMBL WORD COUNTER
WORD COUNTER
DATA CHANNEL CONTROLS
TRAILER TIME 1-SHOT
READY S/R/W
ADR ACKNOWLEDGE
LOG ADR INTLK
CYL ADR BUS
UPPER HEAD SELECT
SECTOR ADDRESS BUS
SECTOR NOTCH
PSEUDO-SECTOR OSC
READ CLOCK
(SERIAL) WRITE DATA & CLOCK
(SERIAL) READ DATA
SEL UNIT 1
SEL UNIT 2
SEL UNIT 3
SEL UNIT 4
READ GATE
WRITE GATE
DISK CONTROLLER OVERVIEW

The input to the adder initially is 16_8 from the P.S. Counter and 2 from the mode input. The two LSB's of the P.S. Counter are used (=2) when subtracted this gives Ø i.e. in pseudo sector zero. When a carry occurs from the divider the counter is incremented by one. The sector change F/F also sets which presets the divider to 260 again.

When the correct sector is reached the sector sync logic sets the preamble time F/F (this will not happen if the Disc Change F/F is set). This allows a status to occur and the write clock generator to start sending clock pulses to the drive down the data and clock line. The clock also allows the bit clock to start. The Bit Counter counts 16 bits to make up one word. The carry from the bit counter steps the preamble word counter every other carry. This four bit counter is preset to Ø6 and so counts 12_8 or 10_{10}. This is 16 x 2 x 10 x 640 uS = 240 uS for the preamble time.

As soon as there is a carry from the preamble word counter a data bit is put onto the line to the drive. There is a sync bit for read purposes. Data is now shifted out from the shift register and is put on the line as required. The word counter, preset to complement of record length, counts the length of the record. As well as putting data on the line the data also goes into the check register to form the checksum. As soon as the word counter overflows, the check word time F/F is set which gates the data in the check register to the drive. When the checkword has gone a 20 uS trailer time monostable is fired. This keeps clock bits going onto the disc to allow time for the erase head to go past the check word.

When start occurs 3 data channel cycles follow which fill up SR, DRB and DPA. When DRA becomes empty a further DCH cycle occurs which fills it up again.

Done sets at the end of trailer time and generates an interrupt so that the controller can be set up again as soon as possible.

Read

When sector sync occurs the Preamble time F/F sets as before and enables the Read delay counter. This counts 4½ pseudo oscillator pulses (4½ x 20 = 90uS) and then enables read status. The read data is then fed into the read data latch logic which shapes the pulses coming in and makes them the correct width. As soon as the first data bit is found (this is the sync bit put on at the end of the preamble during write) the clock is fed into the bit and word counters to count the correct data time. The data is shifted into the shift and check registers and then via DRA and DRB to the memory with a DCH cycle. After data time the check word from disc is put into the check register and the resulting output should be zero.

Check

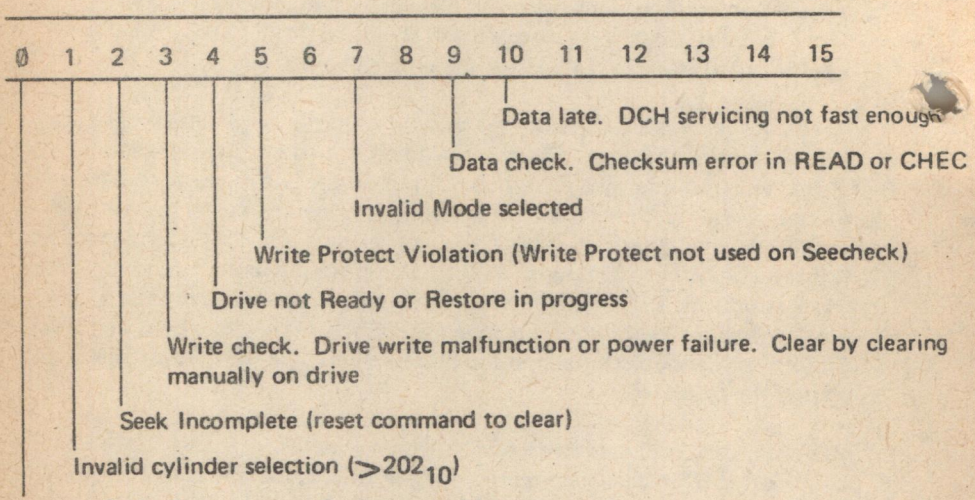
This operation is the same as for read except that no DCH cycles take place.

Reset

A restore signal is issued to all drives to drive the heads to track zero.

DIA

This is used to input the current status of the disc controller held in the ending status register (ESR) and would be used after every read or write to check that no errors had occurred.


Ø 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
Data late. DCH servicing not fast enough
Data check. Checksum error in READ or CHEC
Invalid Mode selected
Write Protect Violation (Write Protect not used on Seecheck)
Drive not Ready or Restore in progress
Write check. Drive write malfunction or power failure. Clear by clearing manually on drive
Seek Incomplete (reset command to clear)
Invalid cylinder selection (>202_{10})
Unusual End. One or more of other error bits set.

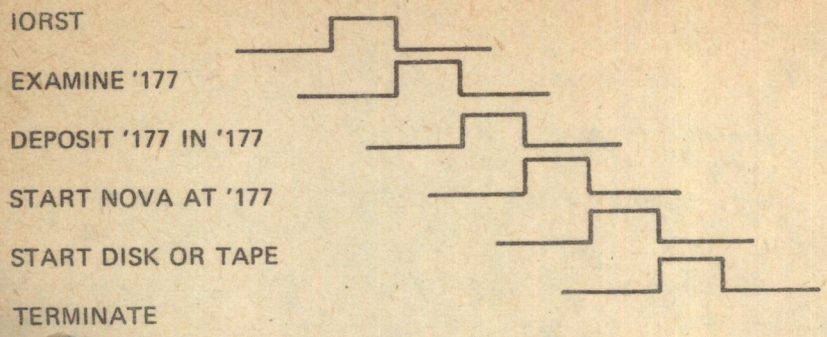
DIB

This is used to input the current state of the core address register set up by the DOB.

Cold Start

This enables the record at Sector Ø track Ø to be read from Disk or the first record to be read off tape. The data read in is known as a bootstrap as it enables the rest of the software on disk or tape to be read in. The bootstrap is 200_8 long to overwrites core locations Ø -177_8.

The cold start enable switch enables the special logic on the control panel to be gated onto the I/O lines. When the Disk or Mag tape cold start switch is activated the following sequence takes place.



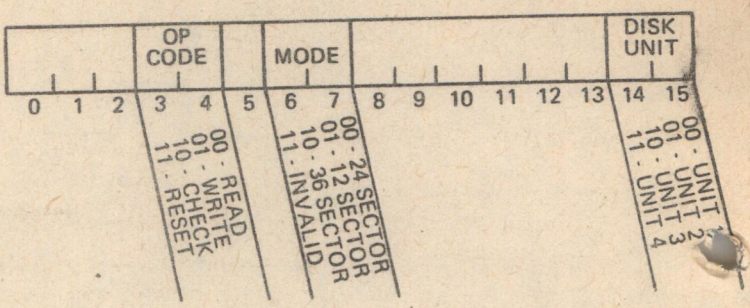
The Nova loops on the JMP 177 until the Data channel has read in 200 words and overwrites 177. 177 now contains a Jump into the bootstrap.

The cold start enable switch must be reset to allow control panel switch data to be read into the Nova.

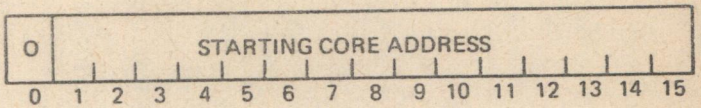
The software term 'Disk Warms' is the same thing as Disk cold start.

DISK CONTROLLER ACCUMULATOR CONTENTS

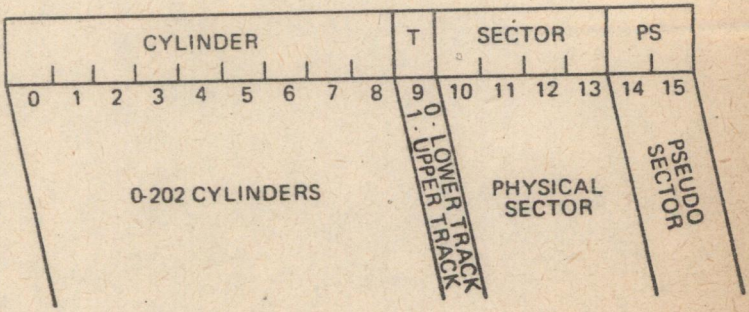
DOA, AC, 32


OP CODE
MODE
DISK UNIT
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
00 - READ
01 - WRITE
10 - CHECK
11 - RESET
00 - 24 SECTOR
01 - 12 SECTOR
10 - 36 SECTOR
11 - INVALID
00 - UNIT 1
01 - UNIT 2
10 - UNIT 3
11 - UNIT 4

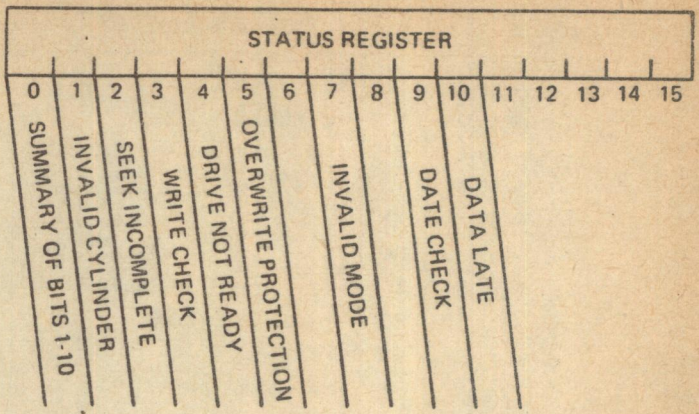
DOB, AC, 32



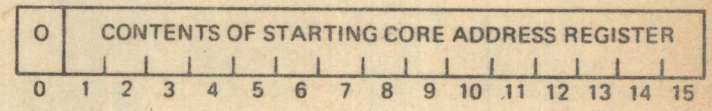
DOC, AC, 32



DIA, AC, 32


STATUS REGISTER
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
0 SUMMARY OF BITS 1-10
1 INVALID CYLINDER
2 SEEK INCOMPLETE
3 WRITE CHECK
4 DRIVE NOT READY
5 OVERWRITE PROTECTION
7 INVALID MODE
9 DATE CHECK
10 DATA LATE

DIB, AC, 32



DIABLO INTERFACE CONNECTOR PINS

Signal Function		Pin	Signal Function		Pin
Track Address	– bit 1	LL	Sector Mark		W
	– bit 2	N	Index Mark		Y
	– bit 4	RR	Sector Address	– bit 1	CC
	– bit 8	J		– bit 2	JJ
	– bit 16	XX		– bit 4	KK
	– bit 32	FF		– bit 8	MM
	– bit 64	T		– bit 16	UU
	– bit 128	BB	*Pseudo Sector-Mark		S
Restore		VV	Write Check		HH
Strobe		SS	Read Clock		A
Head Select		AA	Read Data		C
Write Gate		EE	Read Gate		E
Write Data and Clock		B	Select Line	– Unit 1	L
*Write Protect Input		H		– Unit 2	R
*Write Protect Status				– Unit 3	V
Indication		P		– Unit 4	Z
*Erase Gate		K	*High Density Indication		M
File Ready		U	**Daisy Chain Cable		
Ready to Seek, Read or Write		F	Terminator, +5		PP
*Address Acknowledge		NN	Ground		D
*Logical Address Interlock		XX	Ground		DD
Seek Incomplete		TT	Ground		WW

*Related to optional features

**Pin (PP) supplies +5 volts to the cable terminator network

DIABLO POWER CABLE

	Pin
Ground	C
+15V ± 5%	K, H
-15V ± 5%	R, P

NOTE: These pins are at the Diablo end of the power cable. For more complete data refer to pages 2–4, 5 & 6.

Test Point	Location	Function	Ref. Sheet
1	L5	+GO	1
2	D6	+DATA TIME	1
3	K5	-READ DATA	2
4	M7	-SER WR DATA	2
5	K6	+BIT TIME Ø	2
6	X6	-PSEUDO SECTION MK	5
7	F5	-DSK DCHA	9
8*		-INDEX MARK	3
9*		-SECTOR NOTCH	5

Not fitted on boards manufactured prior to PC artwork revision B.

Table 1 : Test Points

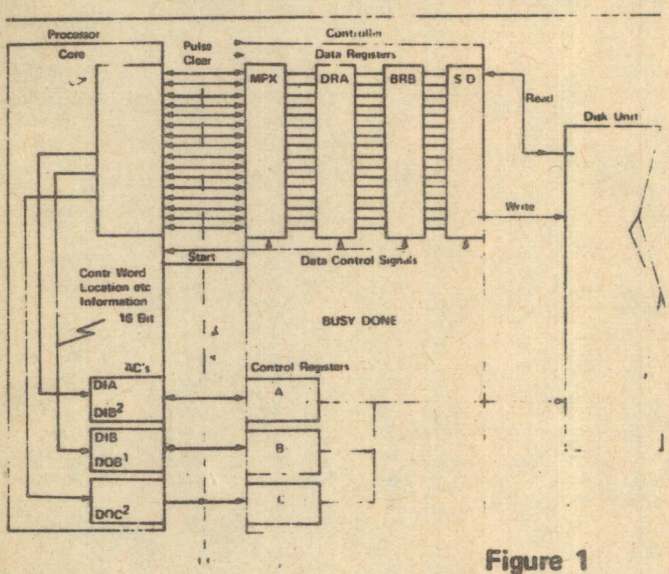


Figure 1

Functions Bits 8,9

01 = "S": START — The disk operation is started, and proceeds according to the initial contents of the disk controller's registers. "Busy" is set; "Done" and pending disk interrupts are cleared.

10 = "C": CLEAR — The disk operation, if extant, is stopped. "Busy", "Done" and pending disk interrupts are cleared. Disk controller register contents remain undisturbed.

11 "P": PULSE — No function.

Signal Name	Logic Diagram Sheet & Edge (L, R)	Mother-Board Connector	Pin	Processor (Amphenol #17-10500) Connector Pin	Flat Cable (ref. Fig. 16) Cable#	Color	Drive Winchester #MRAC-42.. Connector Pin
- ADR BIT 1	1 R	A	81	6	1	Brown	LL
2	1 R	A	85	7	1	Red	N
4	1 R	A	84	8	1	Orange	RR
8	1 R	A	87	9	1	Yellow	J
16	1 R	A	86	11	1	Blue	X
32	1 R	A	89	12	1	Violet	FF
64	1 R	A	88	13	1	Gray	T
128	1 R	A	91	14	1	White	BB
256	1 R	A	90	38	4	Green	(unassigned)
- RESTORE	1 R	A	73	5	3	Green	VV
- ADR STROBE	1 R	A	71	1	3	Brown	SS
- UPPER HEAD	3 R	A	83	47	2	Gray	A
- WR PROTECTED	4 L	A	78	48	2	White	P
- WR DATA & CLOCK	2 R	A	63	10	1	Green	B
- ERASE GATE	(see note)	—	—	—	—	'Erase Gate' not used. Tie to pin EE at Drive.	K
- WR GATE	1 R	A	75	39	4	Blue	EE
- DRIVE RDY	4 L	A	79	40	4	Violet	U
- READY S/R/W	1 L	B	38	41	4	Gray	F
- ADR ACKNOWL-EDGE	1 L	A	59	42	4	White	NN
- LOG ADR INTL'K	1 L	A	57	45	2	Blue	XX
- SEEK INCOMPLETE	4 L	A	76	44	2	Green	TT
- SECTOR NOTCH	5 L	B	23	4	3	Yellow	W
- INDEX MARK	3 L	A	69	18	2	Brown	Y
- SECT ADR BIT 1	5 L	B	51	34	4	Brown	CC
2	5 L	B	11	35	4	Red	JJ
4	5 L	B	15	36	4	Orange	KK
8	5 L	B	13	37	4	Yellow	MM
- WRITE CHECK	4 L	A	77	3	3	Orange	HH
PSEUDO-SECT OSC	5 L	B	19	33	3	White	S
- READ CLOCK	2 L	A	67	31	3	Violet	A
- READ DATA	2 L	A	65	20	2	Orange	C
- READ GATE	1 R	A	61	2	3	Red	E
- SEL UNIT 1	3 R	B	31	19	2	Red	L
2	3 R	B	34	21	2	Yellow	R
3	3 R	B	25	30	3	Blue	V
4	3 R	B	27	32	3	Gray	Z
- SEL FIXED PLTR	3 R	B	36	46	2	Violet	(un assigned)
GROUND				22			D
GROUND				25			DD
GROUND				26			WW
GROUND				29			—

Table 2: Signal/Control Cable, Processor ⟷ Drive

'H' = High-active signal
'L' = Low-active signal
'B' = Bidirectional bus line
'D' = From processor to device
'P' = From device to processor

Signal	Level	Direction	Back-Panel Pin	Controller Logic Page, Edge
CLR	H	D	A50	4L
DATA0	L	B	B62	Note 2
DATA1	L	B	B65	
DATA2	L	B	B82	
DATA3	L	B	B73	
DATA4	L	B	B61	
DATA5	L	B	B57	
DATA6	L	B	B95	
DATA7	L	B	B55	
DATA8	L	B	B60	
DATA9	L	B	B63	
DATA10	L	B	B75	
DATA11	L	B	B58	
DATA12	L	B	B59	
DATA13	L	B	B64	
DATA14	L	B	B56	
DATA15	L	B	B66	
DATIA	H	D	A44	4L
DATIB	H	D	A42	4L
DATIC	H	D	A54	Note 1
DATOA	H	D	A58	4L
DATOB	H	D	A56	4L
DATOC	H	D	A48	4L
DCHA	L	D	A60	9L
DCHI	H	D	B37	9L
DCHMO	L	P	B17	9R
DCHMI	L	P	B21	Note 1
DCHO	H	D	B33	9L
DCHP IN	L	D*	A94	9L
DCHP OUT	L	D*	A93	9R
DCHR	L	P	B35	9R
DSO	L	D	A72	4L
DS1	L	D	A68	4L
DS2	L	D	A66	4L
DS3	L	D	A46	4L
DS4	L	D	A64	4L
DS5	L	D	A64	4L
INTA	H	D	A40	9L
INTP IN	L	D*	A96	9L
INTP OUT	L	D*	A95	9R
INTR	L	P	B29	9R
IOPLS	H	D	A74	Note 1
IORST	H	D	A70	4L
MSKO	L	D	A38	9L
OVFLO	H	D	B39	Note 1
RQENB	L	S	B41	9L
SELB	L	P	A82	4R
SELD	L	P	A80	4R
STRT	H	D	A52	4L
COLD STRT	H	D	A49	4L

*For the two pairs of priority-determing signals, the in signal comes from the processor or the preceding device, the out signal goes to the next device. If the computer is operated with an interface board removed (or a slot is not used), jumper pin A93 to A94 and A95 to A96 to maintain bus continuity.

NOTES

1. Line not used by Disk Controller II.

2. Data Bus lines drive on logic sheets 14, 6, 8, & 9; sampled on sheet 16.

Table 3

DIABLO DISK DRIVE

The Disc

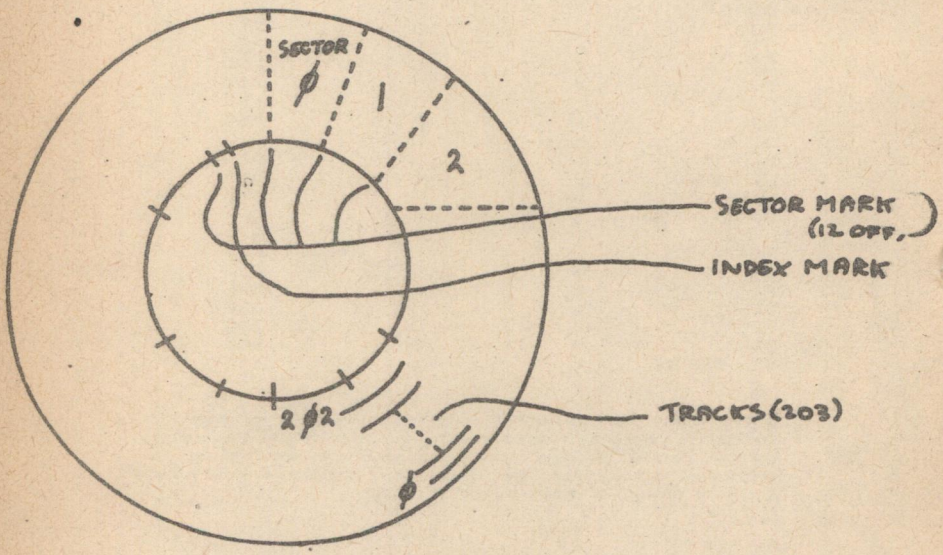
The Diablo drive uses a single platter disc which is held in a plastic cartridge for ease of transport and interchangeability. Upon insertion the disc is held magnetically so that it can rotate freely within the cartridge. Two models are in use 31 and 33, both basically the same.

There are two heads, one for each surface which perform the read, write and erase functions. Recording is done by saturating the metal oxide coating in one direction or the other.

The disc is split up into 12 sectors (single bay) or 24 sectors (double bay). The sectors are defined by notches cut into a ring attached to the disc. The 12 sector disc is further divided electronically into 24 or 36 sectors. The division into 12 by the notches is called physical sectoring, and the division into 24 or 36 is called pseudo sectoring. The 24 sector mode is used in the normal running of the Seecheck system.

A further notch is cut to give a reference point for sector zero, this is known as the Index mark.

Forming concentric circles around the disc are the tracks or cylinders. There are 203 tracks per surface.

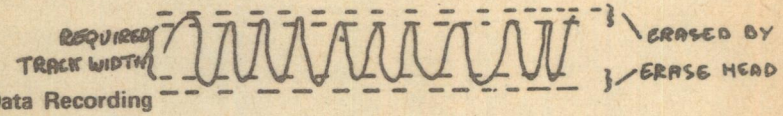


The Head

The read/write/erase head passes over the recording surface at a distance of 80u inches from the surface. This distance is maintained by the shape of the flying head and the airflow over it, which is governed by the speed of rotation (1500 r.p.m. = 1%).

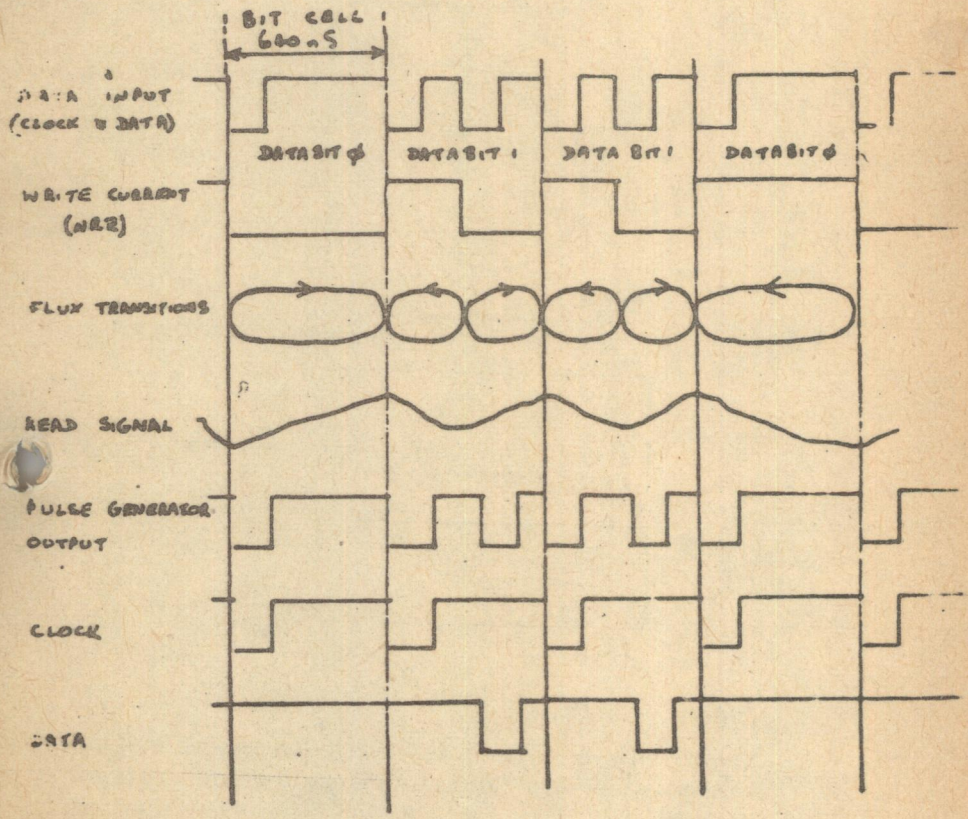
As the head gets nearer to the centre of the disc the relative speed of the disc is lower and so the head gets nearer to the surface. A decrease in write current has to take place when this point is reached

The erase head is behind the write head and erases the sides of the track written by the write head.



Data Recording

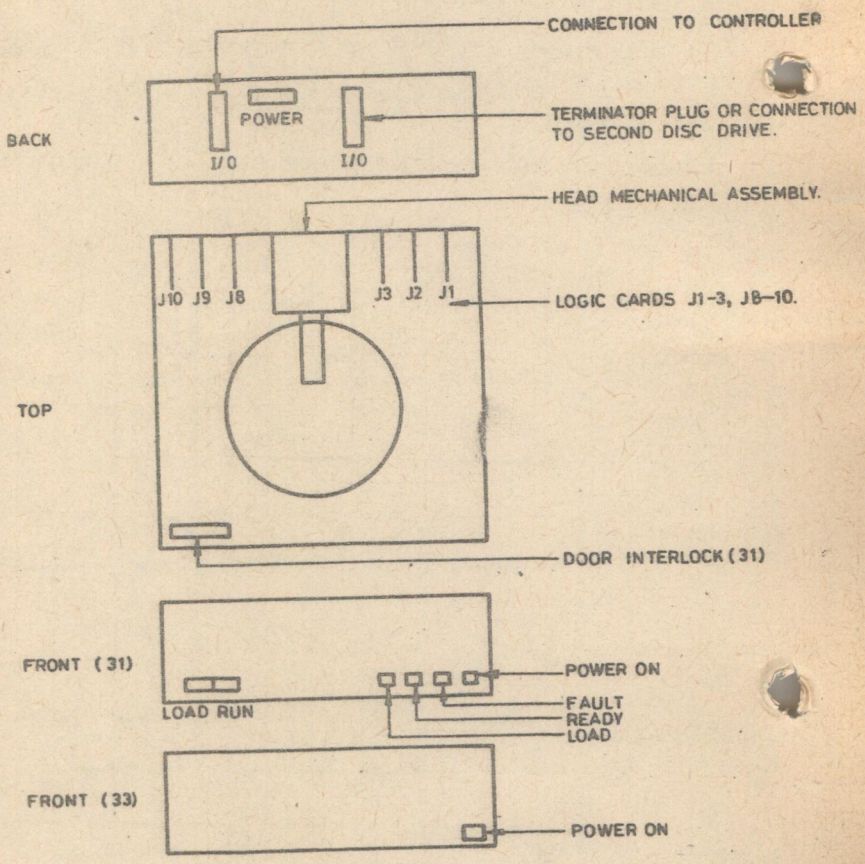
Data is written onto the surface using non return to zero (NRZ) recording



The number of 16 bit words written per sector depends on the sector configuration.

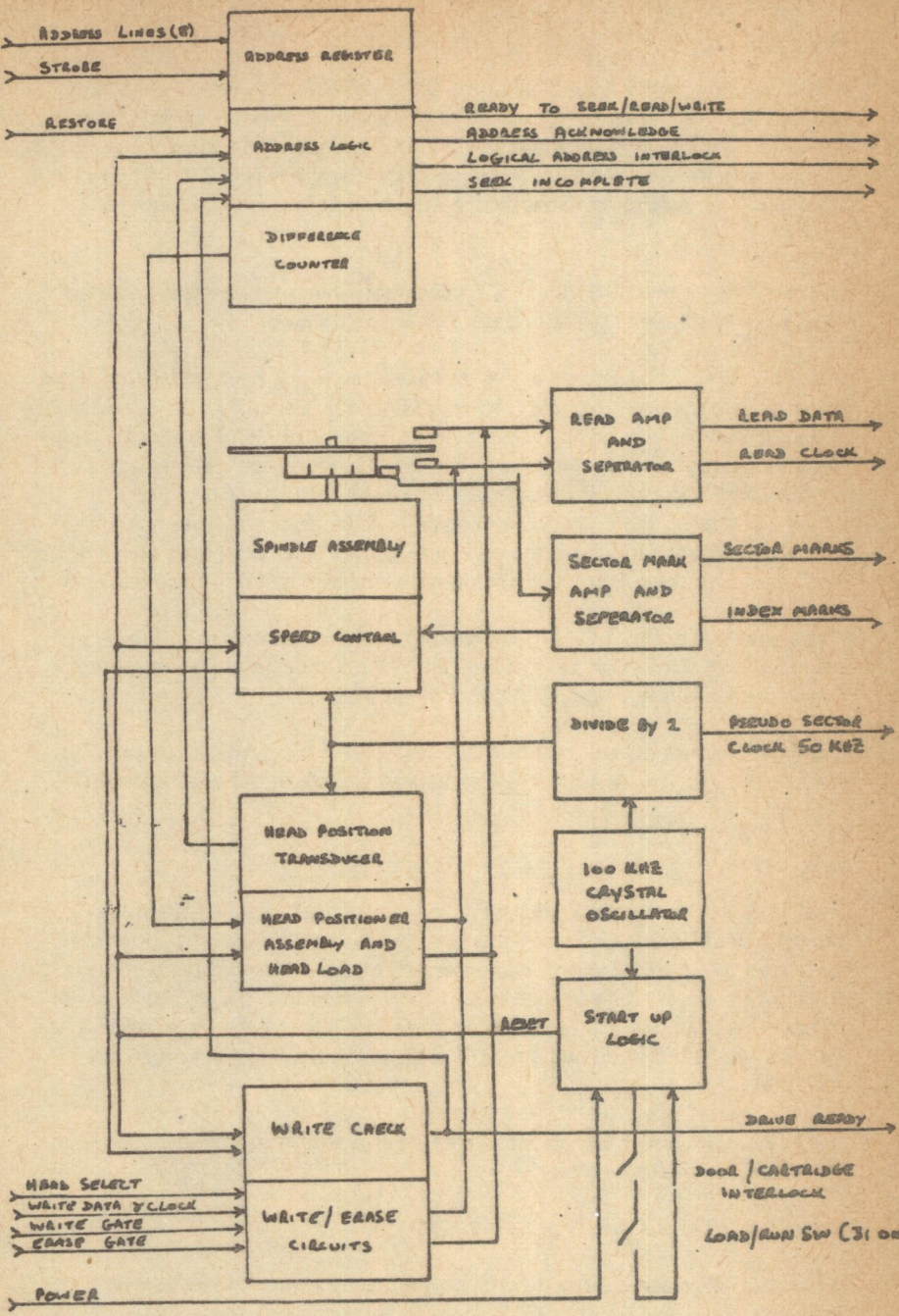
12 sectors	400_8	= 256 words
24 "	200_8	= 128 "
36 "	100_8	= 64 "

Physical Layout



Power

The disc drive requires only +15v, −15v and Ground. This is supplied from a Dynage power supply located at the rear of the bay and to the left of the disc drive.


ADDRESS LINES (8)
STROBE
RESTORE
ADDRESS REGISTER
ADDRESS LOGIC
DIFFERENCE COUNTER
READY TO SEEK/READ/WRITE
ADDRESS ACKNOWLEDGE
LOGICAL ADDRESS INTERLOCK
SEEK INCOMPLETE
READ AMP AND SEPERATOR
READ DATA
READ CLOCK
SPINDLE ASSEMBLY
SPEED CONTROL
SECTOR MARK AMP AND SEPERATOR
SECTOR MARKS
INDEX MARKS
DIVIDE BY 2
PSEUDO SECTOR CLOCK 50 KHZ
HEAD POSITION TRANSDUCER
HEAD POSITIONER ASSEMBLY AND HEAD LOAD
100 KHZ CRYSTAL OSCILLATOR
ABET
START UP LOGIC
WRITE CHECK
DRIVE READY
DOOR / CARTRIDGE INTERLOCK
LOAD/RUN SW (31 ONLY
HEAD SELECT
WRITE DATA & CLOCK
WRITE GATE
ERASE GATE
WRITE/ ERASE CIRCUITS
POWER

DESCRIPTION

Power On

If the switch is in the LOAD position (31) then when power is applied the address counter is reset to zero and the heads are restored to track Ø. When the head has stopped the door unlock solenoid is energised and the door can be lowered and the disc cartridge removed (31). On the model 33 the drive has to be slid backwards and the top cover removed before the door can be opened.

NOTE: On the model 33 there is no automatic restore to zero so the head must be pushed back manually before lowering the door.

If the switch is RUN on power on, or the switch is put from LOAD to RUN the heads are restored to zero. The spindle motor is energised at low drive and after about 15 seconds the motor is switched into high drive and runs up to about 1800 rpm. The heads are then lowered into their operating position and high drive switched out. When the speed has slowed to just below 1500 rpm high drive is cut in again and the disc drive goes ready and can accept a command from the controller. When the speed goes above 1500 rpm again high drive is cut out, the speed being controlled in this manner =1%.

If the switch is put to LOAD (31) the motor drive is removed, the heads unloaded and restored to zero. When all motion has ceased the door unlock solenoid is energised enabling the door to be opened.

If the restore should fail, the door will not open if the heads are beyond about track 10. This is controlled by a microswitch on the head end stop.

Seek

To initiate a seek the track address is put on the lines and a strobe pulse issued. The difference between the new address and the current address is calculated by an adder and the complement of the difference loaded into a difference counter. The new address is then loaded into the address counter and address acknowledge sent back to the controller. If the track address is > 202 seek is inhibited and a logical address interlock signal sent to the controller.

The head drive motor is then set in motion at one of 4 speeds, depending on the difference in the counter.

Speed 4 = >32, 3 = >8, 2 = >2, 1 = >Ø.

When the difference is Ø the head is within 3/8 of a track of the correct track position.

Whilst the head is in motion the ready to the controller and write are inhibited.

ack Counting and Final Positioning

ıe track counting is controlled by a transducer which consists of two glass ›re discs on which have been etched a square wave pattern. One disc is fixed d the other rotates as the head moves. A 50KHZ triangular waveform is d to the moving disc. When stationary over a track the two etches exactly atch and the induced output in the fixed disc is a maximum. When the ad moves, the etches are displaced and the induced signal decreases to a inimum and then increases to a maximum in the other direction.

hen the signal has decreased and returned to a maximum in the original rection, one track movement has taken place. This 1 track displacement is d to s[illegible] difference counter. When the difference counter reaches zero the rvo motor control brings the head to a halt by reaching the nearest maximum gnal peak.

rite check

ıe write check light is illuminated and a write check signal sent to the ›ntroller if there is:–

1) A malfunction in the write circuit.

2) A malfunction in the erase circuit.

3) Supply voltage less than 13.5 volts.

CB Functions

1
- Head position servo
- Motion detector

2
- Difference counter
- Speed and direction control
- Restore control

3
- Address register
- Address arithmetic
- Adder
- Command sequencing

8
- 100 KHZ oscillator
- Position transducer driver
- Lamp drivers (Ready and Check)
- +5V regulator drive
- -15V voltage low sensing
- Sector address and Index drive to controller

J9	Sector and Index amplifier and separator Start up control Speed control Head load Door unlock 100 KHZ divide by two
J10	Head select Write amp Read amp Erase driver Read seperator Write check

Heat Sink Assembly

Motor drive transistors
+5V regulator transistor
Head drive transistor

MAINTENANCE

Every 3 months.

Clean heads and inspect for scratches and oxide build up.

Clean disc surface and inspect for scratches.

Clean generally.

If wick on carriage rail is white apply 1 drop of oil.

Renew air filter.

MAGNETIC TAPE

MAGNETIC TAPE

Data is stored on tape 7 or 9 bits at a time. This is made up of 6 or 8 data bits plus a parity bit. Odd or even parity can be specified. There are three models in use.

1. Bucode. Model 2015–001 and 2015–002. The 2015–001 was fitted to the earlier double bay systems and has a different load/unload procedure.

   Tape speed is 25 i.p.s.

   9 track model density 800 b.p.i. NRZ1

   7 track model density 800 or 556 b.p.i. NRZ1

   Both 7 and 9 track have a HI/LOW density switch but it is only operative on the 7 track drive.

2. Pertec Model 6840/9 and 6840/75

   Speed and Density the same as for Bucode which it replaces on the Redifon systems.

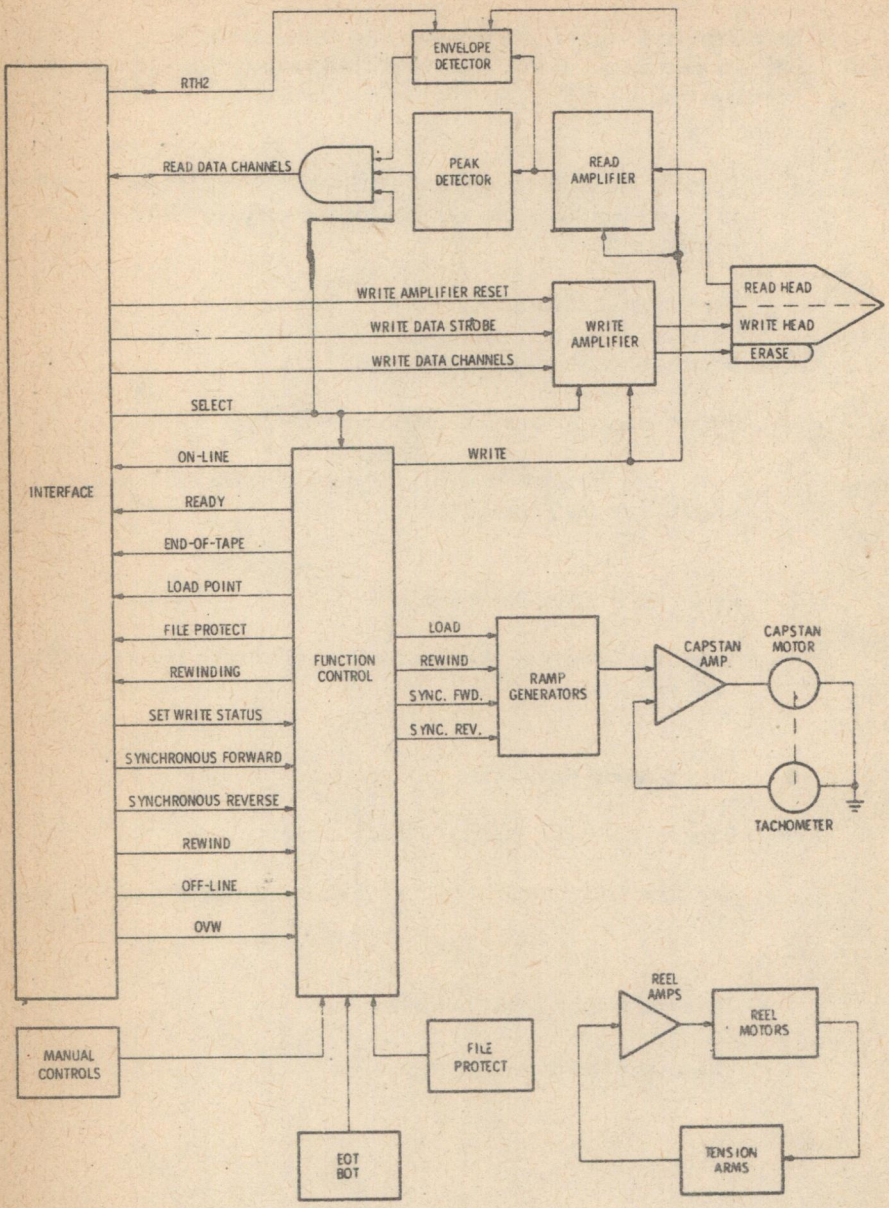
3. Pertec. Model 6640/9/25

   9 track 1600 b.p.i., 25 i.p.s: Phase encoded.

   The drive has a formatter with it which is mounted beneath the disc drive.

4. Tesla and Aritma Tape Controllers

   The description is given on page 4–64.

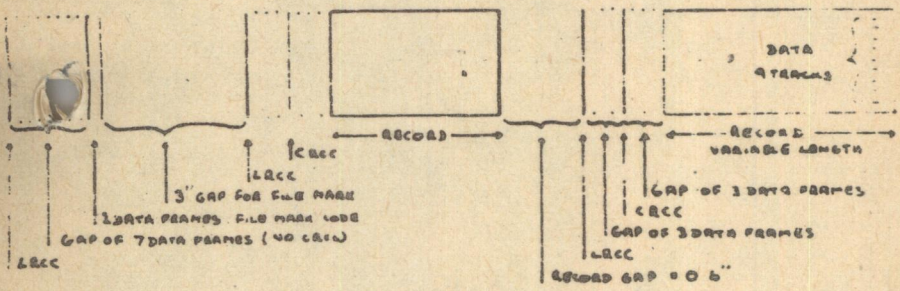


Block Diagram of Model 6640 Tape Transport

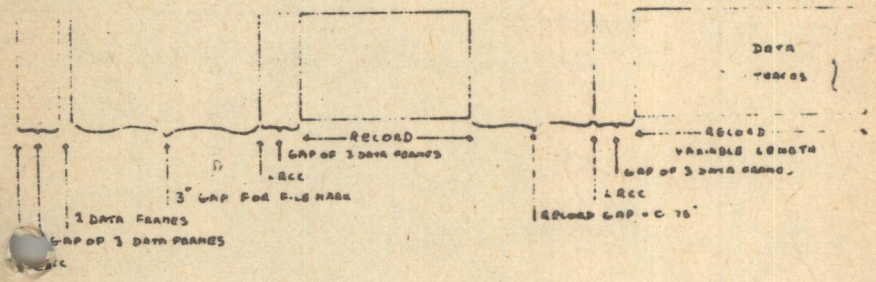
Tape Format

To ensure that tapes can be transferred to another system it is essential that the deck is set up correctly. An IBM master skew tape, which has data written on it at the correct frequency and position, is used to set up the deck.

9 TRACK 800 bpi



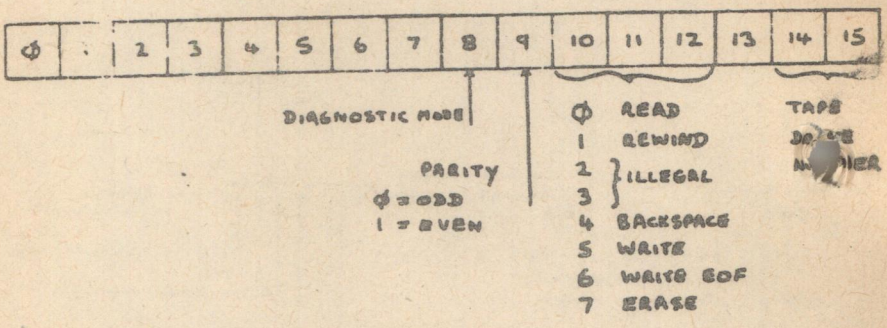
1 TRACK 800/556 bpi



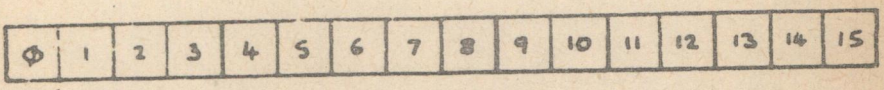
Tape Controller Set Up

The Controller is set up using the three commands DOA, DOB, DOC.

DOA SET MODE

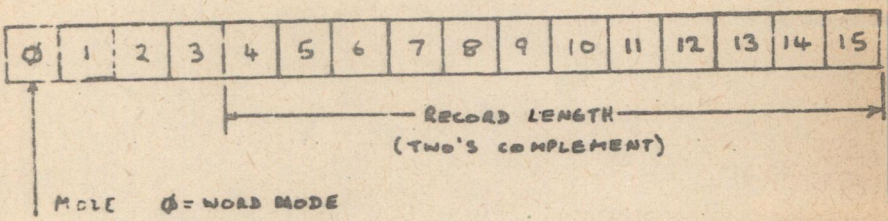


DOB SET DCH CORE ADDRESS

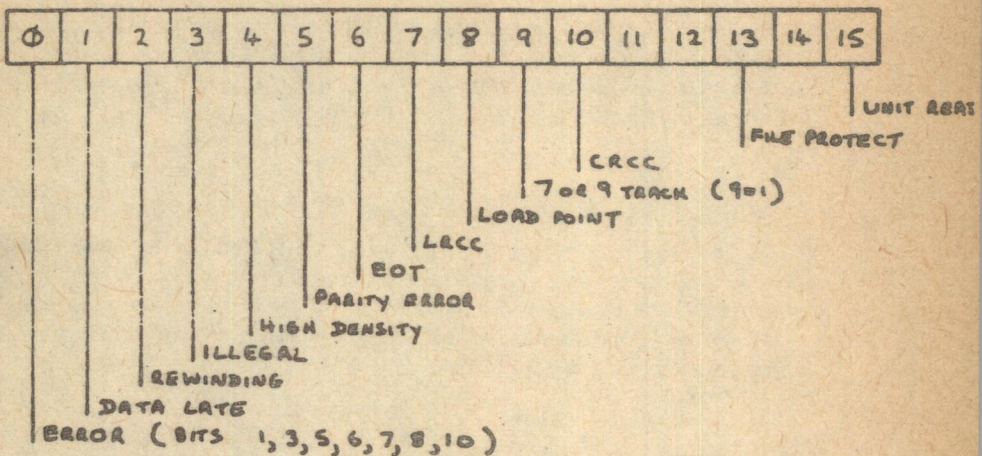


0 : 0-32K STARTING ADDRESS OF BLOCK TRANSFER IN MEMORY. REGISTER INCREMENTS AFTER EACH TRANSFER.

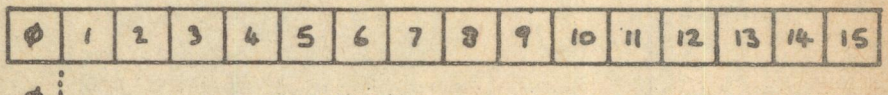
DOC SET RECORD LENGTH



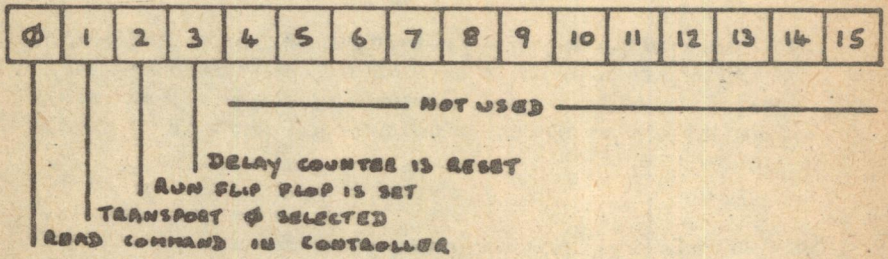
DIA INPUT STATUS REGISTER



DIB INPUT CORE ADDRESS REGISTER



DIC DIAGNOSTIC MODE


0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
NOT USED
DELAY COUNTER IS RESET
RUN FLIP FLOP IS SET
TRANSPORT 0 SELECTED
READ COMMAND IN CONTROLLER

WRITE

Start

DOA, DOB and DOC are issued from the CPU to set up the various conditions. Included in the DOC is a start command. The start F/F is set and this sets the RUN F/F which in turn enables forward motion to the drive. The start F/F also initiates the first DCH cycle.

DCH cycle

RQENB (Request enable) from the CPU sets DCHR (Request). When DCHA (Acknowledge) is received, provided the controller still has priority, the address is put on the line and the Mode bit set to zero (memory output mode – read). When the CPU sends CHO the address is removed from the line and the data strobed into the data buffer.

Start Up delay

The start F/F sets SIB (start if beginning of tape) or SIN (not beginning) this enables a delay counter which counts pulses from the main clock generator. When the correct delay decode is reached ADT (allow data transfer) is set which enables the to be strobed to the drive, SIN or SIB is reset which holds the delay counter reset. ADT also enables read data strobes from the drive (read afterwrite).

Data Transfer

Control of the 8 bits to the drive is by the ODD F/F which either gates the L or R half of the word to the drive. Bits 0–7 are sent first, then 8–15 when the ODD F/F sets. The setting of ODD also initiates another DCH cycle. The ODD F/F is set and reset by write Strobes.

Parity

The 8 bits are fed through a parity generator which provides 9th bit for the drive. Odd or even parity can be specified. Note that when reading the presence of a bit of data on the tape provides a read strobe. If even parity is used then the software must ensure that there is at least one bit in the 9 bit frame on the tape.

CRCC (9 track only) Cyclic redundancy check character

As the data is transferred to the drive it is also manipulated (exclusive or of old and new data with a shift) into a 9 bit CRCC register

End of Write

When the length counter has reached maximum (loaded with 2's complement of record length) it resets ADT and sets WCC F/F (write check character). The delay counter is started and after 3 frame times the CRCC character is sent to the drive. After a further 3 frame times WAR (write amp reset) is sent to the drive which causes the LRCC character to be written into the tape. WAR resets WCC F/F which resets and stops the delay counter.

Tape Stop

The last read data strobe (read after write) triggers the IRG (inter record gap) monostable. After a delay of 800 uS this times out setting EOR (end of record). This sets TOD (Turn off delay) and TAD (turn around delay) which starts the delay counter. When the delay is decoded TOD is reset and stop generated, which resets run, which stops the forward motion, resets busy and sets done.

Turn Around Delay

After the 3 MS TOD, TAD is not reset until a further 12 mS have elapsed. If during this 12 mS another command is issued (Busy is reset so this is permissible), then if it is in the same direction and mode (e.g. read followed by read) TAD is reset before the 12 mS by start and start is allowed to set run again. If it is a different command (e.g. read followed by write), then the 12 mS elapses before TAD is reset and run is then allowed to set.

Read

The read is very similar to write with the following exceptions.

DCH cycle

The mode bit is a 1. CHI is sent from the CPU and the data for memory is put on the line. The first DCH cycle occurs when the ODD F/F is set for the first time.

Data Transfer

The ODD F/F is set and reset by Read data strobes.

Parity

The incoming data is put into the parity generator which compares the output with the parity bit from the drive. A F/F is set if an erro occurs.

CRCC (9 track only)

The incoming read data is manipulated into the CRCC register. When the CRCC frame strobed in the output should be zero. A F/F is set if an erro occurs.

The incoming read data is exclusive or 'd with the LRCC register. After th LRCC frame has been strobed in the output should be zero. A F/F is set i an error occurs.

End of Read

When the last read data strobe has occurred a monostable times out aft 2½ frames. The next read data strobe is used to strobe the CRCC fram in. A second monostable then times out for a further 2½ fram[illegible] follow which the next read data strobe is used to strobe the LRCC ch[illegible]ter i 800 uS later the IRG monostable times out and the drive stops in the s way as for write.

Erase

The erase is similar to write with the following exceptions.

DCH Cycle

There are no DCH cycles.

Start up delay

This is 140 mS (write is 24 mS).

Data Transfer

There is no data transfer. As soon as ADT has set it sets EOR. [illegible] erase used to provide the 3 inch gap for a file mark.

End of File

WEF (Write end of file) is identical to write except that the CRCC charac is not written at the end.

The software is set up for a one word transfer. This one word is a special code.

Start is set but run does not set. RTP (rewind tape) is set which resets B RTP sends a Rewind Command to the drive and the resets. The Drive

rewinds at fast speed.

A rewinding signal is sent from the drive which can be examined by software with a DIA, input status register.

Backspace

Backspace sets reverse motion. When IRQ is detected the drive stops in the same way as for write.

Illegal Commands

When ILC is set it sets EOR. The end is then the same as for write. ILC is set by:

1. One of the two illegal commands in the DOA word.
2. Backspace command issued whilst at load point.
3. A write command issued whilst file protect is on.

Busy must be reset by the software before ILC can be reset with the next start pulse.

2 MODELS

1.	Model 6640	9 track	25 i.p.s.	6640/9/25.
	9 track	1600 b.p.i.	25 i.p.s.	Phase encoded

The drive has a formatter which is mounted.

2.	Model 6840/9	9 track	25 i.p.s.
	/75	7 track	25 i.p.s.

Adjustments for the two models differ slightly. In the cases where the adjustments are different, both sets of adjustments are given under the respective model heading.

BLOCK DIAGRAM

Tape Control System

When LOAD control is depressed first time, K1 relay is energized, the four contacts close, activating the reel servos which tension the tape, closing the tension arm limit switch. The relay is latched so that it remains activated after LOAD control is released. The contact K1D closes, INTLK level goes high removing reset signal from control flip flop.

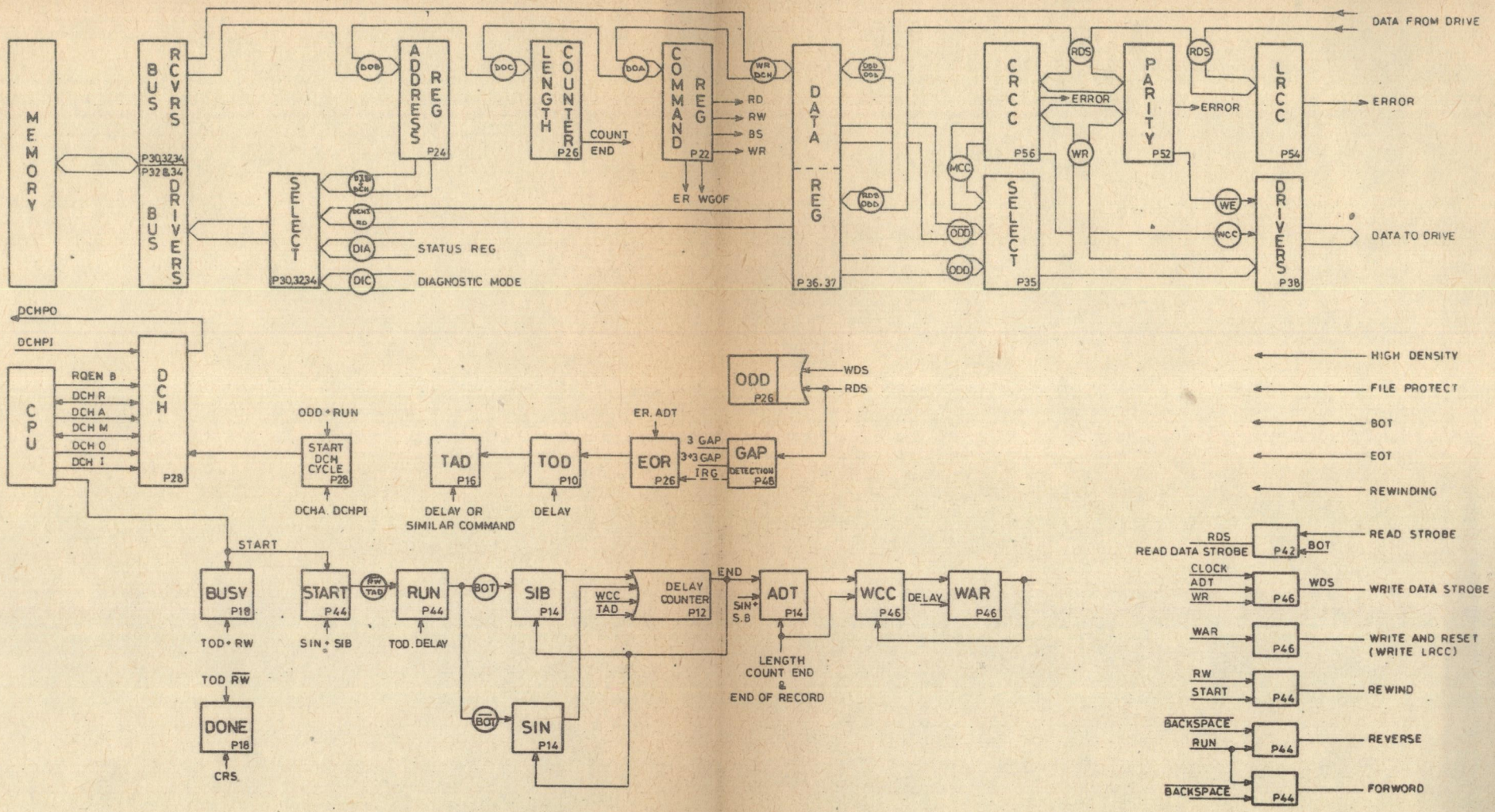
When the LOAD control is depressed a second time, INTLK signal is still high and U18 and U31 flip flops are set. The Q output of U18 is fed to one input of U21 OR gate. Output of U21 goes low which enables the FORWARD RAMP GENERATOR that drives the Capstan servo. The tape moves forward until BOT tab reaches BOT sensor. BOT signal goes high enabling one input of AND gate U29. The single shot is also triggered generating 0.5 second negative-going waveform (NBOTD) AND gate U29 is enabled, and the load flip flop (U18) reset, the tape will stop with BOT under sensor, U41 has at present all three inputs high, therefore NLDP is low, showing transport is at Load point and enabling the load lamp driver.

After the 0.5 second delay, NBOTD goes high, NBUSY is high and output of U30 is high, therefore output U38 (AND) low which enables one input of AND gate U39.

Flip flop U31 has been set causing NFLR to go low disabling AND gate U10 and disables any further LOAD COMMAND.

Depress On-Line Control

ON-LINE control is depressed, on-line flip flop U26 is set (if it is depressed a second time, U26 is reset), which enables the second input of AND gat



BLOCK DIAGRAM
7or 9 Track Tape Controller

U39. $\overline{Q}$ out of U26 enables the ON-LINE lamp driver. U39 output goes high indicating transport is ready and on-line (RO). If transport is also selected output of U40 goes high (SRO), and NON-LINE at gate U12 disables the rewind control.

ISLT (Interface Select Transport) is low when transport is selected.

When FLR or INTLK are low, gates U23, U24 hold on-line flip flop U26 reset, ensuring on-line flip flop cannot be set until the interlock has been made and the FIRST LOAD REWIND sequence has been entered. On-line flip flop can also be set from the interface by the (OFFC) off-line command via U22 and U24. The transport is now ready to receive external commands.

Operation from CPU

With the tape unit selected, ready and on-line (SRO is high), if ISFC (Interface Synchronous Forward Command) is received output of U4 goes high and output of U6 goes low, MOTION signal goes high and the FORWARD RAMP GENERATOR is enabled through U21.

The MOTION signal is delayed 10 u secs, differentiated and a positive going pulse is generated (GO). If ISWS (Interface Set Write Status) is true, write/read flip flop U20 is set and NWRT goes low. If ISWS is false, flip flop U20 is reset and NWRT goes high.

Normal Rewind

On a rewind command, RW1 flip flop is set, Q output goes high enables rewind ramp generator via gate U28. RW3 flip flop $\overline{Q}$ is high. Tape accelerates to a reverse velocity of 150 i.p.s. RW1 Q output makes gate U33 output go low which disables U38 and SR0 goes false.

When BOT tab is detected, flip flop RW2 is set on the leading edge of the BOT waveform, RW3 is set on the trailing edge and the 0.5 second single shot is triggered. The $\overline{Q}$ output of flip flop RW3 goes low disabling gate U28. U28 output goes high disabling REWIND RAMP GENERATOR.

At the end of 0.5 second delay the trailing edge of NBOTD is differentiated by S2 generating a positive going pulse (BOTDP) load flip flop U18, is set via gates U9 and U11, enabling FORWARD RAMP GENERATOR.

Note: On rewind the BOT tab overshoots the sensor and then returns.

Data Recording (Write)

If transport is selected, ready, on-line and has a Write Enable ring installed. WRT PWR control line will therefore be at +5v, providing power for the head driver circuits.

When a synchronous forward command is received MOTION signal generated on the Tape Control board goes high, removing one input of gate U8.

The front edge of the SFC is delayed and differentiated, the resulting pulse samples SWS line. If this is true:–

1. The Write/Read flip flop U20 is set.
2. NWRT goes low.
3. Erase driver Q3 is energized.
4. U4 is reset.
5. U9 flip flop is unchanged.

WRITE DATA (WD) input is true (low) enables one input of U2 AND gate. The output of U2 AND gate is applied to J input of U4 (write waveform generator) flip flop and to the K input via U3. U4 is toggled whenever the IWD signal is true.

ISDS is also fed to U9 flip flop which is set on the trailing edge, the Q output unclamps the oscillator which generates a series of pulses, which are fed to the shift register, produces 10 negative going pulses on 10 wires.

The nine outputs T1 to T9 toggle the write waveform generator flip flops (U4 typically), T10 resets U9 flip flop ending the sequence.

Both outputs from U4 are fed to the driver transistors Q1 and Q2, and current will flow in one half or the other of the centre-tap head winding.

In a 9 track system both a CRCC and LRCC are written.

The CRC character is supplied by the customer to the interface, together with a single WDS signal whose trailing edge is separated by four character times from the trailing edge of the last WDS (Write Data Strobe). The LRC character is written by resetting all the write waveform generator flip flops, using the WRITE AMPLIFIER RESET signal. The timing of the reset operation is controlled by leading edge of WARS signal.

U6 output is fed to the OR gate U3, output (positive going) is applied to the K input of U4 and resets U4. The leading edge of the WARS signal is differentiated and sets flip flop U9. A sequence of pulses is produced which toggles the write waveform generator flip flops to the reset state in the appropriate order. The LRCC is written such that the total number of magnetization transitions in any track is even.

In a 7 track system only the LRCC is written.

Overwrite (OVW)

Allows updating (rewriting) of a selected record. The new data block to be inserted must be exactly the same length as the data block being replaced.

The transport must be selected, on-line and a write enable ring installed on the supply reel. The overwrite signal (OVW) from the controller must be true and coincident with SWS and SFC. The operation is terminated by the IWARS signal disabling the write power circuitry.

Read

Data signals from the magnetic head at a level of 10–20mV are fed to the read amplifier. The amplifier output (10.5v model 6840) is full-wave rectified and clipped. The clip level is variable and is under the control of NWRT waveform.

With the transport in the Read mode, NWRT is high and clip level is approximately 20%. The signal is differentiated to form a pulse for each "1" bit detected. This pulse is fed to read statisiser flip flop U14, which is set on the negative going edge of the pulse.

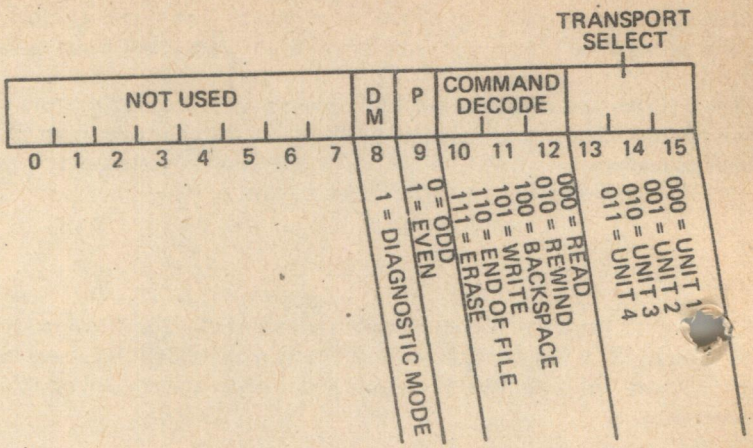
The Q output from U14 is fed to interface driver U16, the $\overline{Q}$ output is fed to the OR gate U11, where it is ORed with the corresponding outputs of the other channels, the first "1" character causes U11 to go high enabling RUN DOWN circuit. At the end of half-a-character period the output goes low. This edge is differentiated by D3 and produces a 2 uS RDS (READ DATA STROBE) pulse fed to CPU.

The output of the rundown circuit is also delayed and resets the read statisiser U14. $\overline{Q}$ output of all the read statisiser flip flops go high and the rundown circuit is therefore clamped. The delay in the loop prevents READ DATA interface lines from resetting before trailing edge of RDS.

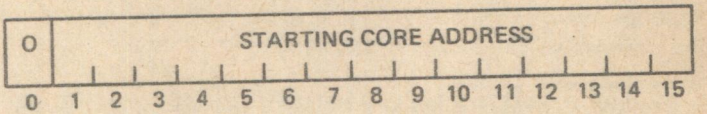
After the last character of a record has been read the SFC goes false, FORWARD RAMP GENERATOR is disabled and the tape decelerates to rest. MOTION signal goes false applying a reset signal to flip flop U14 via U15.

MAGNETIC TAPE CONTROLLER ACCUMULATOR CONTENTS

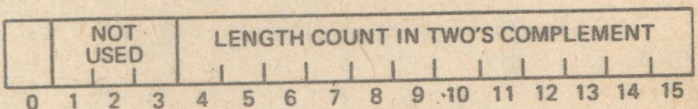
DOA, AC, MTS



DOB, AC, MTS

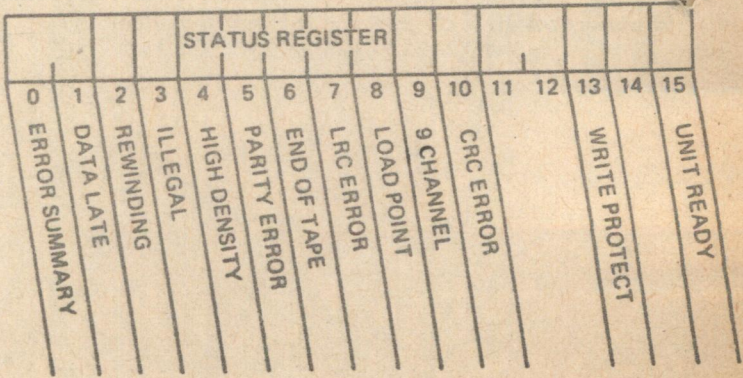


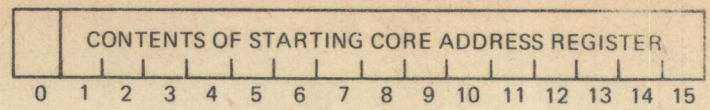
DOC, AC, MTS



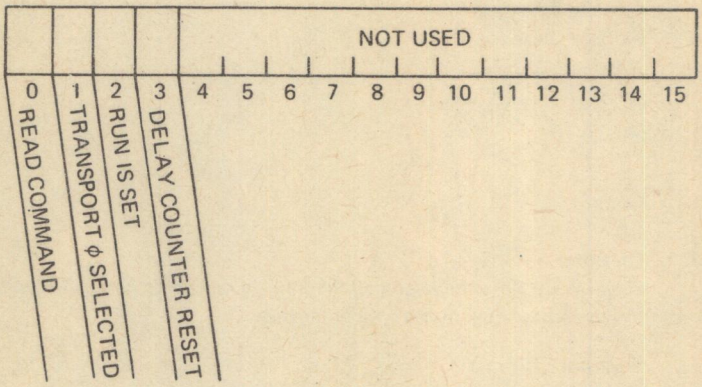
Bit 0 = 1 8-bit characters are counted
Bit 0 = 0 16-bit words are counted

DIA, AC, MTS





DIC, AC, MTS – Diagnostic mode only



MAGNETIC TAPE DEVICE CODES

23 = 7 channel	556 bits/inch	NRZI
23 = 7 channel	800 bits/inch	NRZI
22 = 9 channel	800 bits/inch	NRZI
20 = 9 channel	1600 bits/inch	PE

ALIGNMENT PROCEDURE

TOOLS REQUIRED

1. Entrex Tool Kit
2. Scratch Tape and Write Ring
3. Oscilloscope 432A or equivalent
4. 2 ea x 10 Attenuated Probes
5. 1 ea x 1 Probe
6. Master Alignment Tape
7. Lintless Texwipes
8. Rubber Cleaner
9. Bottle of Glyptal

1. **Cleaning**
   Clean Read/Write head and all metallic guide rollers with a Texwipe.
   Clean capstan roller with rubber cleaner.

2. **Regulator (B5)**
   Check for proper regulated voltages as follows:
   TP1-B5 (REG) = +12 VDC ± 1.2V
   TP3-B5 (REG) = + 5 VDC ± 0.5V
   TP7-B5 (REG) = -12 VDC ± 1.2V

3. **Reel Servo (B1)**
   A. Mount a Scratch Tape and bring to Load Point. Adjust R1-B1 (RS) until the right tape tension arm is near center position. Repeat this procedure for the left tape tension arm using R2-B1 (RS). Should not slam on unload operation.

4. **BOT/EOT**
   A. Manually position BOT foil at EOT/BOT sensor.
   B. Put channel 1 probe on TP2-B7 (RMP) and adjust R2-B7 (RMP) counterclockwise for 0V. Readjust R2-B7 (RMP) clockwise until the test point voltage switches to approximately 4V positive. Rotate R2 an additional one-quarter turn clockwise.
   C. Carry out the same routine for the EOT sensor, adjusting R1-B7 and monitoring TP1-B7 for the threshold between 0V and 4V. As before, add one-quarter of a turn clockwise.

5. **Write Clock Adjustment**

A. Set Write Clock Density switch on B13 (WC) to 800 bpi. Scope TP7-B13 (WC) for 50 μs full cycle period. Adjust R1-B13 (WC) for proper period.

for 7 track 556 bpi systems adjust R1—B13 (WC) for a 72 µS period.

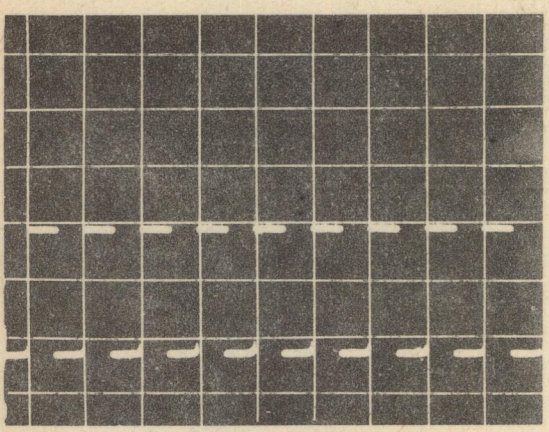


Figure 1

B. **Capstan Adjustment (See page 4—7)** should be done at this point of time.

6. **Forward, Reverse and Rewind Speed**

For: RAMP GENERATOR 501034 or 501840 *only*.

A. Load a Scratch Tape and cycle the MTS up to Load Point (BOT). Depress RESET. Set scope sensitivities to 20 mV/cm. Put channel 1 probe on TP5-B7 (RMP) and adjust R8-B7 (RMP) for OV.

Fine Adjustment – Put channel 1 probe on TP4-B7 (RMP) and adjust R5-B7 for 0V.

B. Put channel 1 probe on TP1-B3 (CA) and adjust R4-B7 (RMP) for 0V.

C. Mount Master Skew Tape for forward and reverse speed adjustments. (Do not use high speed rewind with *Skew Tape.*) Set Off-Line Run switch forward, and measure tape speed at TP3-B14 (RA). Adjust R10-B7 (RMP) forward speed control to obtain a full cycle period of 100 μs, which is 100 μs between positive peaks.

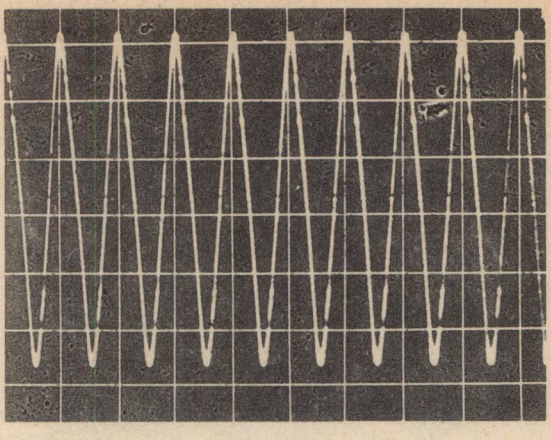


Figure 2

D. Repeat the routine for reverse speed with Off-Line Run switch set to reverse. Adjust R9-B7 (RMP) for a full cycle period of 100 μs at TP3-B14 (RA).

E. Remove the Master Skew Tape. Mount Scratch Tape with Write ring and write a "ones tape" by setting Off-Line Run switch forward, Off-Line Read/Write switch on Write, and Write Clock Density to 800 bpi.

F. Set Scope to 0.5V/Div and 10 μs/Div. Set the three Off-Line switches to neutral and use the "ones tape" to adjust the REWIND operation to six times the speed of forward or reverse. Scope TP3-B14 (RA), hit rewind and adjust R3-B7 (RMP), to produce a full cycle period of 16 2/3 μs or a little less than four positive peaks per 50 μs.

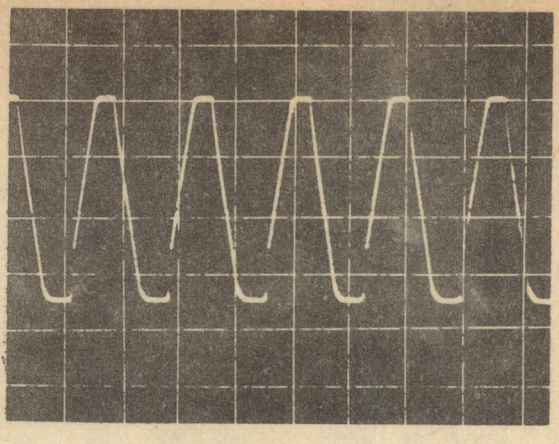


Figure 3

FOR: RAMP GENERATOR 500278 *only*.

A. Load a Scratch Tape, set Off-Line Run switch to neutral, hit RESET, and then adjust R3-B7 (RMP) for 0V at TP3-B7 (RMP).

B. Change scope setting to 0.1V/Div.
Mount Master Skew Tape for forward and reverse speed adjustments. (Do not use high speed rewind with Skew Tape.) Set Off-Line Run switch to forward. Measure tape speed with an oscilloscope at TP3-B14 (RA). Adjust R4-B7 (RMP) to produce a positive sinusoidal peak every 100 μs.

C. Repeat the routine for reverse speed with Off-Line Run switch set on reverse. Adjust R6-B7 (RMP) for a full cycle period of 100 μs at TP3-B14 (RA).

7. Start/Stop Ramp Adjustment

A. Mount a Scratch Tape with Write ring and load to BOT. Hit Remote.

B. Write short records with program on page 4—5 and adjust per step D and step E.

C. Check reverse ramp with location 75=40.

Location	Instruction	
75	000050	Command
76	007775	Word count
77	001000	Buffer
100	020075	Pick up command
101	0610XX	Output it
102	020077	Pick up buffer pointer
103	0620XX	Output it
104	020076	Pick up word count
105	0631XX	Output it and start device
106	0635XX	Busy?
107	000777	
110	010403	Wait loop
111	000777	
112	000766	Back to start
113	000000	Count location
1000	177777	
1001	177777	
1002	177777	

XX = device code (see page 1-7)

C. Set channel 1 probe on TP4-B7 (RMP)

D. START at location 100

E. Adjust R6-B7 (RMP) to 14 ms start time per figure 4.

F. Adjust R7-B7 (RMP) to 12 ms stop time per figure 4.

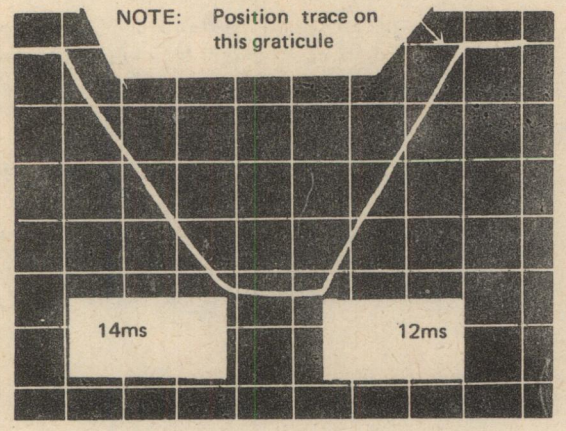


Figure 4

8. **Ferrite Shield Adjustment**

   A. Set Off-Line Read/Write to write, Write Clock Density to 800 bpi and Off-Line Forward/Reverse to neutral. Mount a tape with a Write ring and cycle up to BOT.

   B. Measure the Read Amplifier signals TP3, 6, 9 on boards B14, 15, 16. The crosstalk signal should be less than 300 mV per channel. If excessive crosstalk occurs, reposition the ferrite shield side to side to reduce level of crosstalk (7-channel tape drives have seven test points only).

9. **Read After Write Amplifier Gain**

   A. Load Scratch Tape with Write ring.

   B. Place Write Clock Density switch to 800 bpi, Off-Line Read/Write switch to write, Off-Line Run switch to forward.

   C. Adjust amplifier outputs for 5.5V peak-to-peak as follows:

READ AMP. TEST POINT			
TP3-B14	adjust	R1-B14	
TP6-B14	adjust	R2-B14	
TP9-B14	adjust	R3-B14	
TP3-B15	adjust	R1-B15	
TP6-B15	adjust	R2-B15	
TP9-B15	adjust	R3-B15	
TP3-B16	adjust	R1-B16	
TP6-B16	adjust	R2-B16	Deleted on
TP9-B16	adjust	R3-B16	7-channel drives.

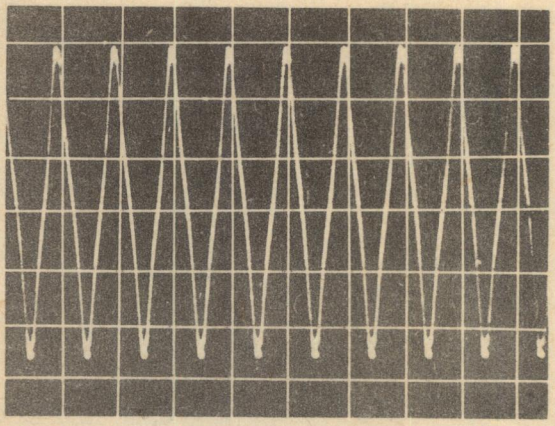


Figure 5

10. **Capstan Tape Walk Correction** (Item 10 should be done before Item 6 page 4–2)
The purpose of this adjustment is to correct the perpendicularity of the capstan with respect to the transport panel.

A. Adjust three capstan adjustment screws (see drawing) such that the capstan mounting plate is approximately 0.090 inch from the rear of the transport panel.

B. Remove inner and outer ceramic guides on both tape guides.

C. Run Tape Transport forward by setting Off-Line Run switch to forward. Adjust forward capstan adjustment screw until the outer tape edge is flush with the outer guide body edges.

D. Run Tape Transport in reverse, and adjust reverse screw until outer tape edge is flush with outer guide body edges.

E. Refine adjustments until no capstan walk is visible and tape edge is flush with outer guide body edges. Tighten adjustment screw lock nuts.

F. Replace ceramic guides and insure that capstan walk is minimal.

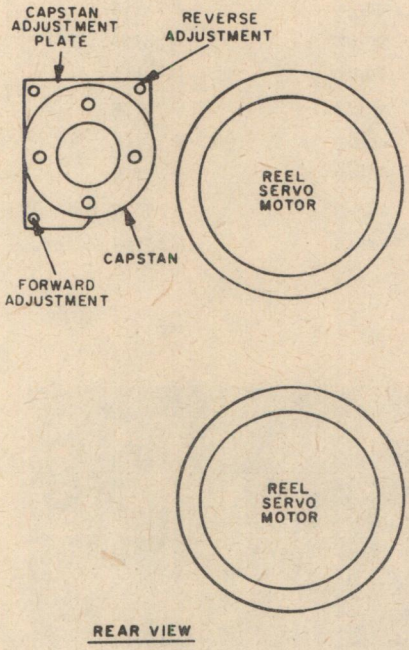


Figure 6

NOTE: Tape Transport door must be fully upright and closed when making static skew adjustment.

A. Set Off-Line Read/Write and Write Density switches to neutral.

B. Demagnetize the Read/Write head.

C. Load Master Skew Tape.

D. Put channel 1 probe on TP3-B14 (RA) and channel 2 probe on TP9-B16 (RA) (TP3-B16 (RA) for a 7-channel drive). External sync probe should be put on TP3-B14 (RA).

E. Set Off-Line Run switch to forward.

Compare channels 2 through 9 to determine that there is not a 360° phase shift between channels 1 and 9 (1 and 7 for a 7-channel drive).

With care readjust the Phillips head and Allen head screws. Proper alignment will produce superimposed signals. To prevent a gross misalignment error of one full bit, observe the alignment of the other Read channels in the Read head: Place scope probe 2 on TP3-B14 (RA) and then scope TP6-B14 (RA), etc. Channel 9 should also superimpose over the Read channel one signal (Channel 7 for a 7-channel drive).

F. Remove Master Skew Tape (do not REWIND, use Off-Line Reverse switch).

G. Skew tolerance is less than 4 μs.

H. Do not overtighten Phillips head screw – use Glyptal to prevent movement of screw.

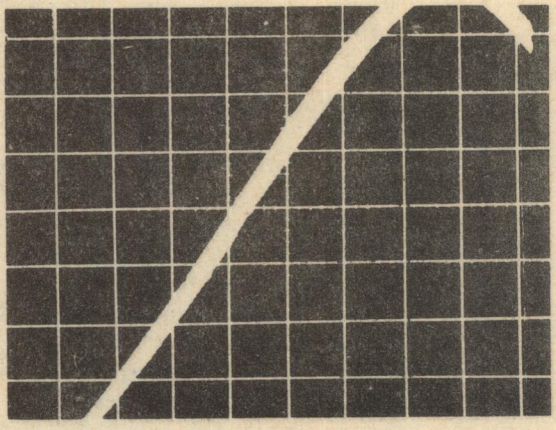


Figure 7

Strobe Adjustment for 9 Channel

Strobe Adjustment for READ after WRITE.

A. Load a Scratch Tape with a Write ring.

B. Scope TP1-A11 (RST).

C. Set Off-Line Read/Write switch to write, Off-Line Density to 800 bpi, and Off-Line Run to forward.

D. Adjust R2-A11 (RST) for a positive pulse of 17.5 μs.

Strobe Adjustment for READ only operation.

E. Use the "ones tape" made in steps A through D to energize the Read head by setting the Off-Line Run switch to reverse.

F. Clear Write Density switch and Off-Line Read/Write to neutral.

G. Adjust R1-A11 (RST) for a positive pulse time of 23 μs.

Strobe Adjustment for 7 Channel

NOTE: All 7-channel drives have the dual density option.

A. Low Density Read
1. Set HI/LO Density switch (on front panel) to LO.
2. Create "ones tape" and mount on tape drive.
3. Read tape by setting the Off-Line Read/Write switch to read and the Off-Line Run switch to forward. Observe TP1-A11 (RST) and adjust R4-A11 (RST) for a 32 μs pulse (556 bpi).

B. High Density Read
1. Set HI/LO Density switch (on front panel) to HI position and create "ones tape".
2. Read tape by setting the Off-Line Read/Write switch to read and the Off-Line Run switch to forward. Observe TP1-A11 (RST) and adjust R1-A11 (RST) for a 23 μs pulse.

C. Low Density Write
Mount Scratch Tape with Write ring.
1. Set HI/LO Density switch to LO.
2. Write tape by setting the Read/Write switch to write, and the Off-Line Run switch to forward. Observe TP1-A11 (RST) and adjust R3-A11 (RST) for a 25 μs pulse (556 bpi).

D. High Density Write
1. Set HI/LO Density switch to HI.
2. Write tape by setting the Off-Line Read/Write to write, and the Off-Line Run switch to forward. Observe TP1-A11 (RST) and adjust R2-A11 (RST) for a 17.5 μs pulse.

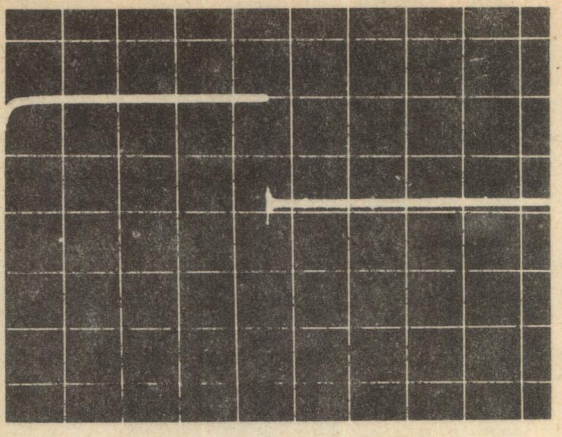


Figure 8

13. Write Symmetry

This adjustment is deleted on some models.

A. Load Scratch Tape with Write ring.

B. Set internal controls as follows:
Off-Line Run – Forward
Off-Line Read/Write – Write
Off-Line Density – 800 bpi

C. Scope test point TP1-A14 (RDO); adjust potentiometer R1-B8 (WA) so that the center pulses approach unity. Maximum tolerance is 6 μs between pulses. Repeat this procedure for the other READ pulse bits.

Test Point READ Pulse Bit		Adjustment Pot.	
A14 (RD)	TP1	R1-B8	
	TP2	R3-B8	
	TP3	R5-B8	
	TP4	R7-B8	
	TP5	R1-B9	
	TP6	R3-B9	
	TP7	R5-B9	
	TP8	R7-B9	Deleted on
	TP9	R1-B10	7-channel drives.

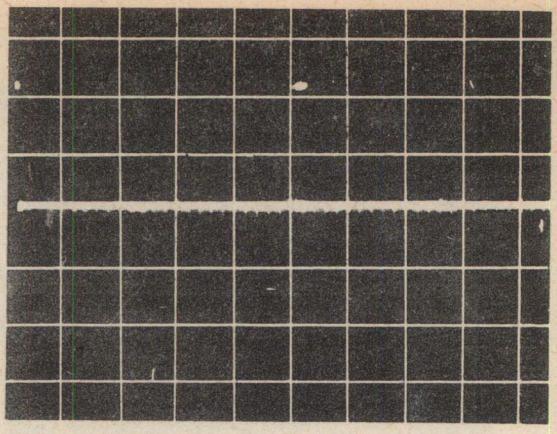


Figure 9

14 Write Skew

A. Load Scratch Tape with Write ring, and turn delay pots: (see table below) fully anti-clockwise.

B. Set Off-Line Run switch to forward, Off-Line Read/Write switch to write and Write Clock Density switch to 800 bpi.

C. Use a two-probe scope technique on the Read Amplifier test points listed to select the Write channel which has the greatest fixed delay. (Latest channel)

D. Place channel 1 probe on this test point as a standard basis of adjustment.

E. Place channel 2 probe on each remaining Read Amplifier test point, increasing each respective delay until each signal coincides in time with the standard signal on channel 1 probe.

WRITE SKEW TABLE

PC Board	Delay Potentiometer	Read Amplifier Test Point	
B8	R2	TP3-B14	
	R4	TP6-B14	
	R6	TP9-B14	
	R8	TP3-B15	
B9	R2	TP6-B15	
	R4	TP9-B15	
	R6	TP3-B16	
	R8	TP6-B16	Deleted on
B10	R2	TP9-B16	7-channel drives.

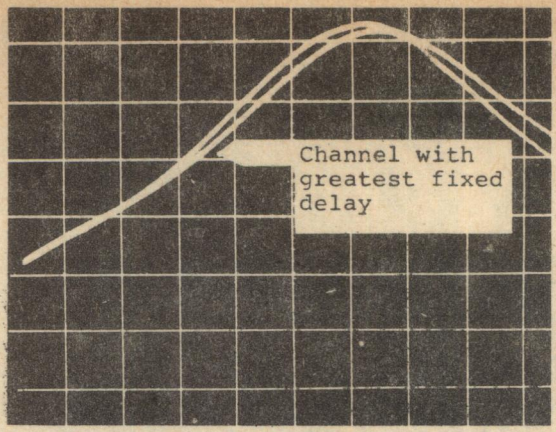


Figure 10

15. Read and Write Threshold Adjust

NOTE: This adjustment is not required on some equipment.

Write

A. Load Scratch Tape with Write ring and hit RESET.

B. Place Off-Line Read/Write to write and Off-Line Run to forward. Place Off-Line Density switch to 800 bpi.

C. Decrease the signal on TP3-B14 (RA) to 3.3V peak-to-peak by adjusting Read Amplifier R1-B14 (RA).

D. Use channel 2 to observe TP1-A14 (RDO) and adjust R2-B13 (WC) until the pulses on scope's channel 2 disappear. Turn R2-B13 (WC) clockwise until one pulse for each positive and negative sinusoidal peak reappears.

Read

E. Create and mount "ones tape".

F. Switch Off-Line Read/Write to read and Off-Line Run to forward.

G. Decrease the signal on TP3-B14 (RA) to 1.6V peak-to-peak by adjusting Read Amplifier R1-B14 (RA).

H. As in step D, use channel 2 probe to monitor TP1-A14 (RDO); then adjust R3-B13 (WC) to threshold (one pulse for each negative and positive peak).

I. Restore R1-B14 (RA) to 5.5V peak-to-peak.

16. Adjustment of File Protect Switch

A. Load a Scratch Tape with a Write ring, and observe if the red File Protect Light goes out. If not, readjust as follows:

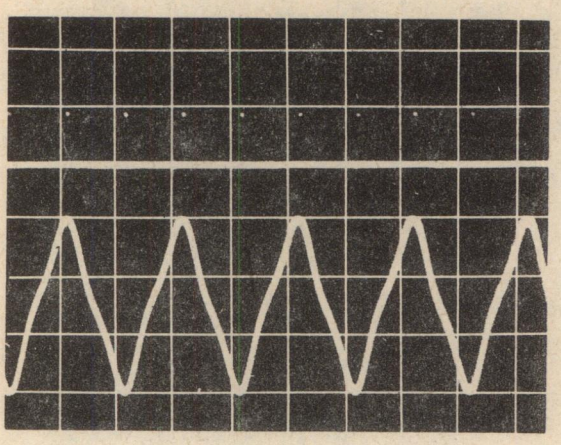


Figure 11-A

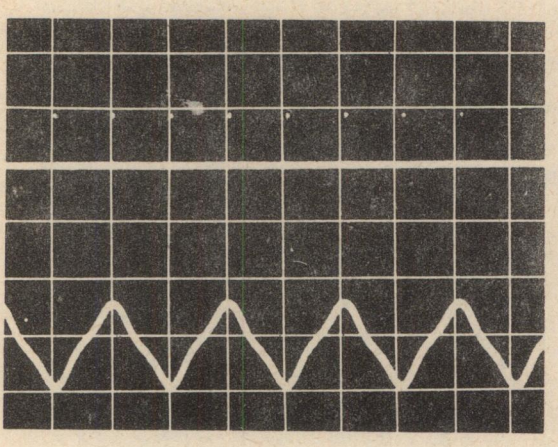


Figure 11-B

B. Loosen the two Phillips head screws supporting the relay. Rotate the relay arm until the relay triggers, causing the File Protect light to go out.

C. Adjust the File Protect Sensing Pin for approximately 1/16 inch clearance from the Write ring. Secure the Phillips head screws.

D. Hit LOAD/UNLOAD and observe the File Protect Sensing Pin moving out when the Reel Servo Tension Arms swing to the off position.

17. Load Cycle Adjustment

A. Load Scratch Tape such that the BOT marker is beyond the EOT/BOT sensor. Scope TP5-B6 and hit LOAD/UNLOAD.

B. Adjust R1-B6 for a search time of 15 sec.

18. Erase Circuit Checkout

A. Make a "ones tape" by setting Off-Line Read/Write to write, Clock Density to 800 bpi, and Off-Line Run to forward.

B. Power down the Tape Transport and remove Write Amplifiers B8, B9, and B10.

C. Refeed the "ones tape" into the Read/Write head with the same switch settings as indicated in step 18A.

D. Test the Read Amp outputs to determine if the erase head is cleaning the tape of old data. The signal strength should be below 50-100 mV peak-to-peak. Restore the Write Amps to the same slots they were removed from.

19. Reel Adjustment

A. Starting from BOT marker on tape, run full reel of tape in forward direction. Check tape stacking on upper reel. Tape should not be touching the outer edges of the reel flanges while stacking.

B. Starting from EOT marker, run full reel of tape in reverse direction. Check tape stack as per step 19A.

C. Determine direction hub must be moved to correct tape stacking. Using 1/8 Allen wrench, with special extension, loosen two set screws on hub. Loosen the set screw located on the shaft flat. Correct hub position and reset the two set screws. The set screw located on the shaft flat should be tightened last. After setting hub, repeat procedures outlined in steps 19A and B.

20. Hub Adjustment

A. If the Reel Servo Hub does not expand sufficiently to make a tight fit with the tape reel, readjust the hub with a 3/16 Allen wrench.

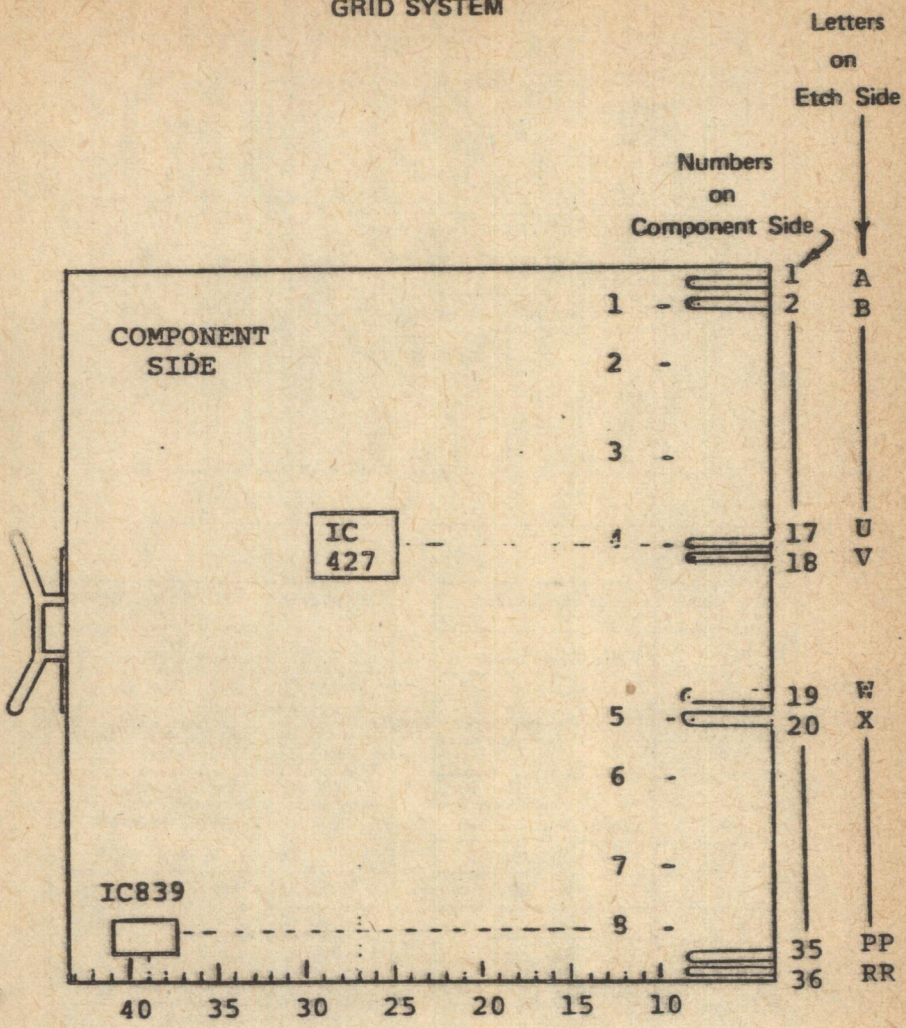
NOTE: The adjustment is located in the center of the Reel Servo Hub.

REPLACEMENT PROCEDURE

Bucode 2015 Printed Circuit Boards

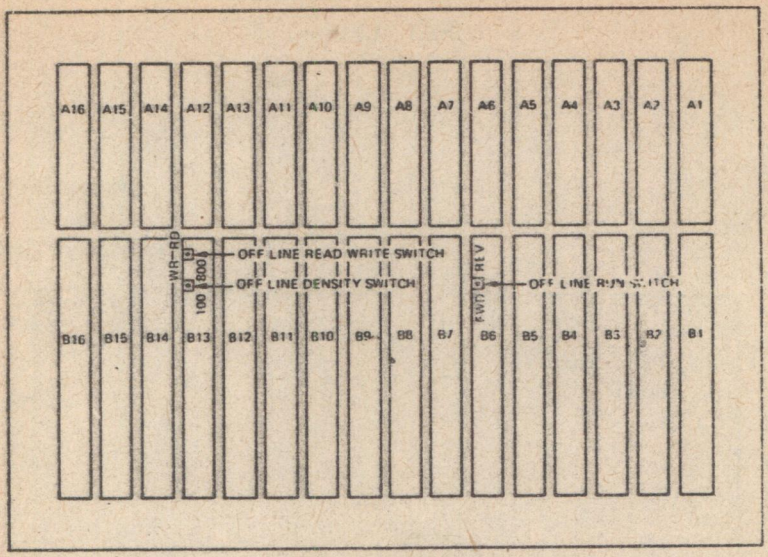
PCB Replaced	Adjustments to be Performed
Reel Servo (B1) RS	3. Reel Servo (B1)
Capstan Amplifier (B3) CA	6. Forward, Reverse and Rewind Speed
Regulator (B5) REG	2. Regulator (B5)
Transport Control (B6) TRC	17. Load Cycle Adjustment
Ramp Generator/Sense Amplifier (B7) RMP	4. BOT/EOT; 6. Forward, Reverse and Rewind Speed 7. Start/Stop Ramp Adjustment
Write Amplifier (B8, B9, B10) WA	9. Read After Write Amplifier Gain (Only needs to be done on those read amplifier outputs which control the channels affected by the replaced write amplifier.) 13. Write Symmetry (where applicable) 14. Write Skew
Amplifier Interface (B12) AIN	NONE
Write Control (B13) WC	5. Write Clock Adjustment 15. Read and Write Threshold Adjust
Read Amplifier (B14, B15, B16) RA	9. Read After Write Amplifier Gain (Only needs to be done on the replacement board.)
Transport Interface (A6) TIN	NONE
Terminator (A7, A12) TRM	NONE
Read Strobe (A11) RST	12. Strobe Adjustment
Read AMP Output (A14) RDO	NONE
Reel Servo Motor	19. Hub Adjustment 20. Reel Adjustment
Tape Tension Arm	21. Tape Tension Arm Replacement
File Protect Switch	16. Adjustment of File Protect Switch
Read Write Head	8. Ferrite Shield Adjustment 9. Read After Write Amplifier Gain 11. Static Read Skew
Ferrite Shield	8. Ferrite Shield Adjustment

BUCODE P. C. BOARD
GRID SYSTEM



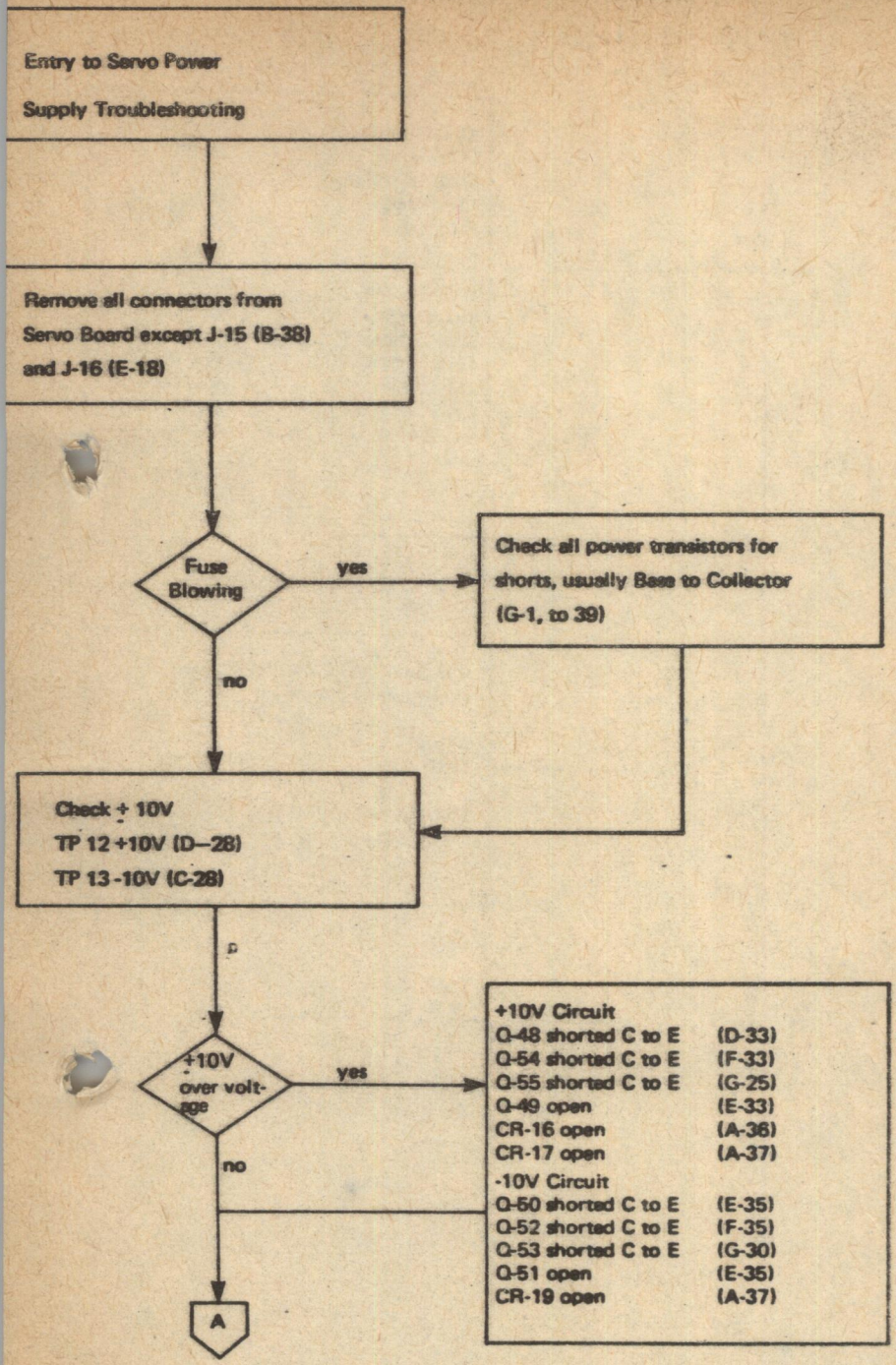
NOTE: On the etch side pins, the letters (G, I, O, Q) are skipped in the numbering sequence.

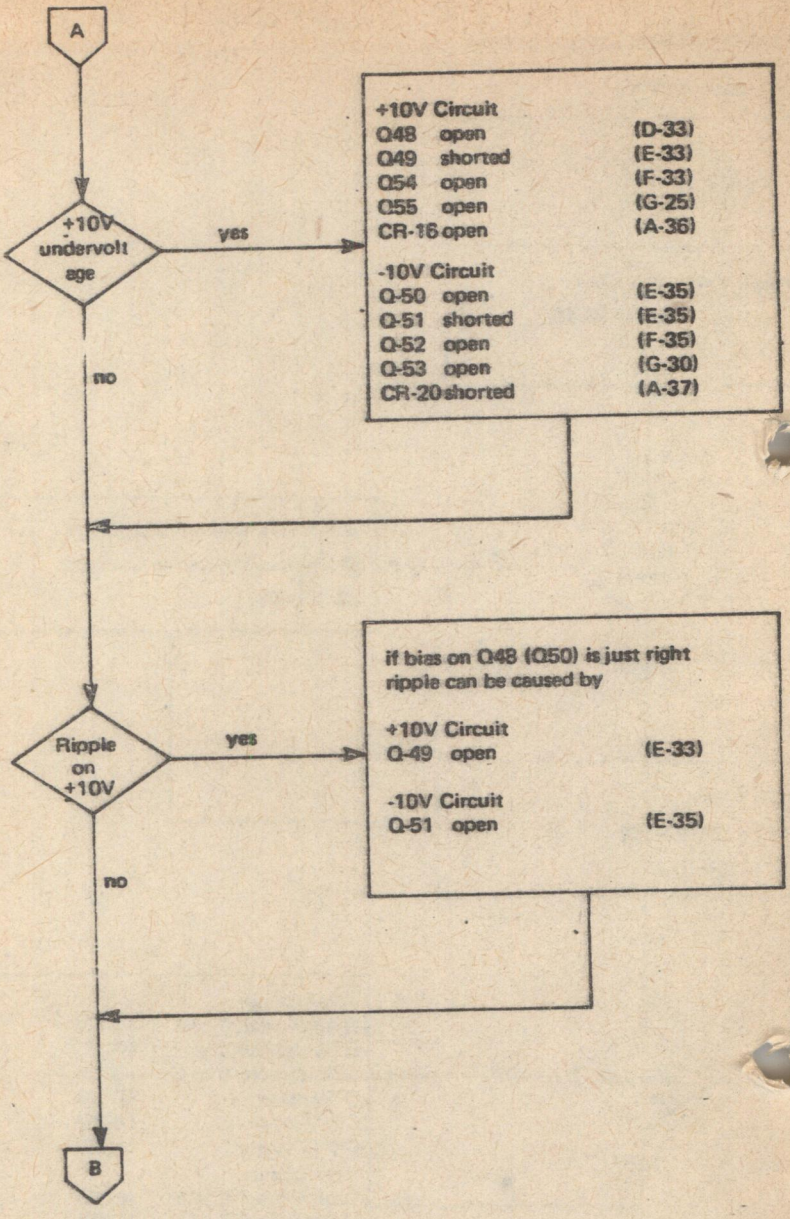
BUCODE PRINTED CIRCUIT BOARD LOCATIONS

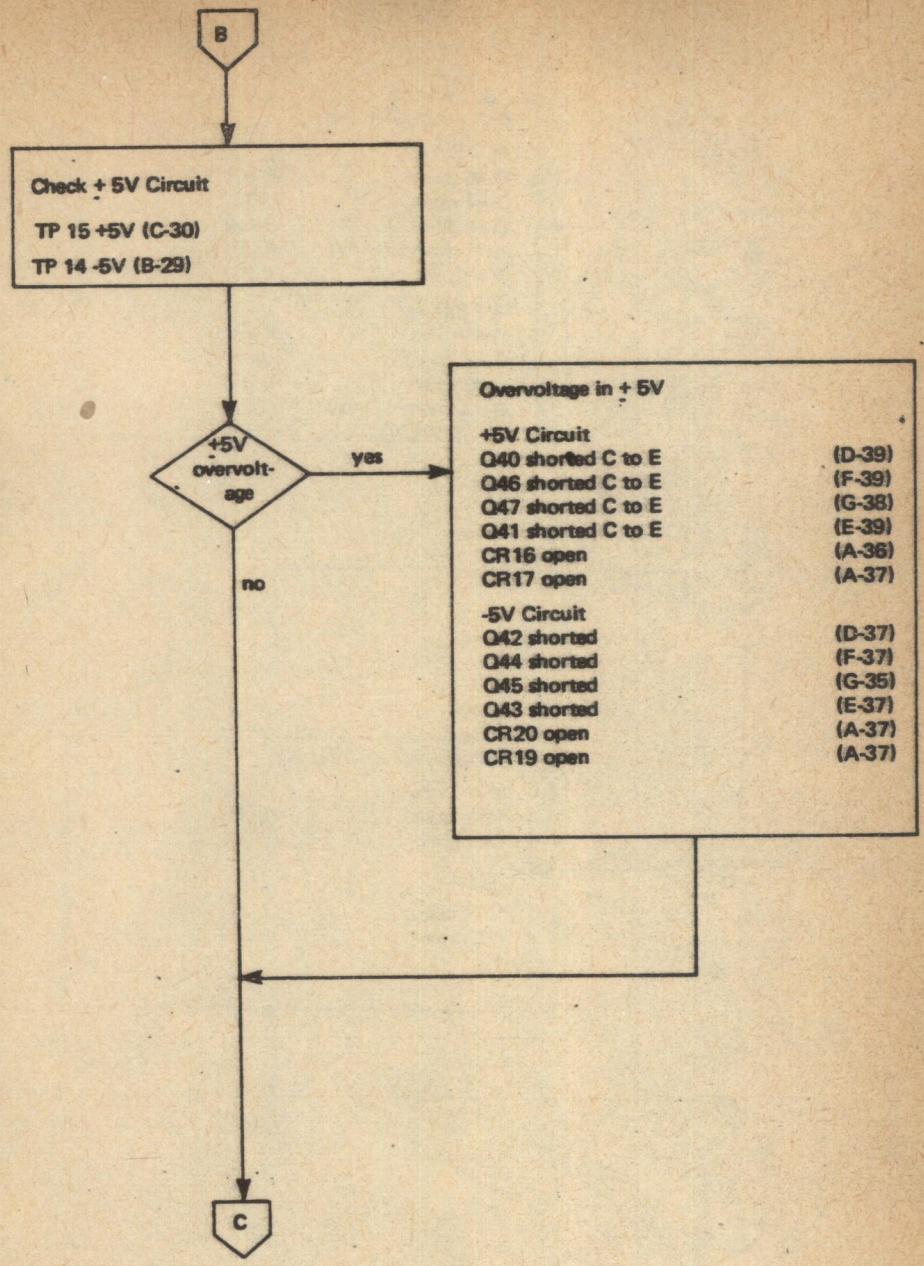


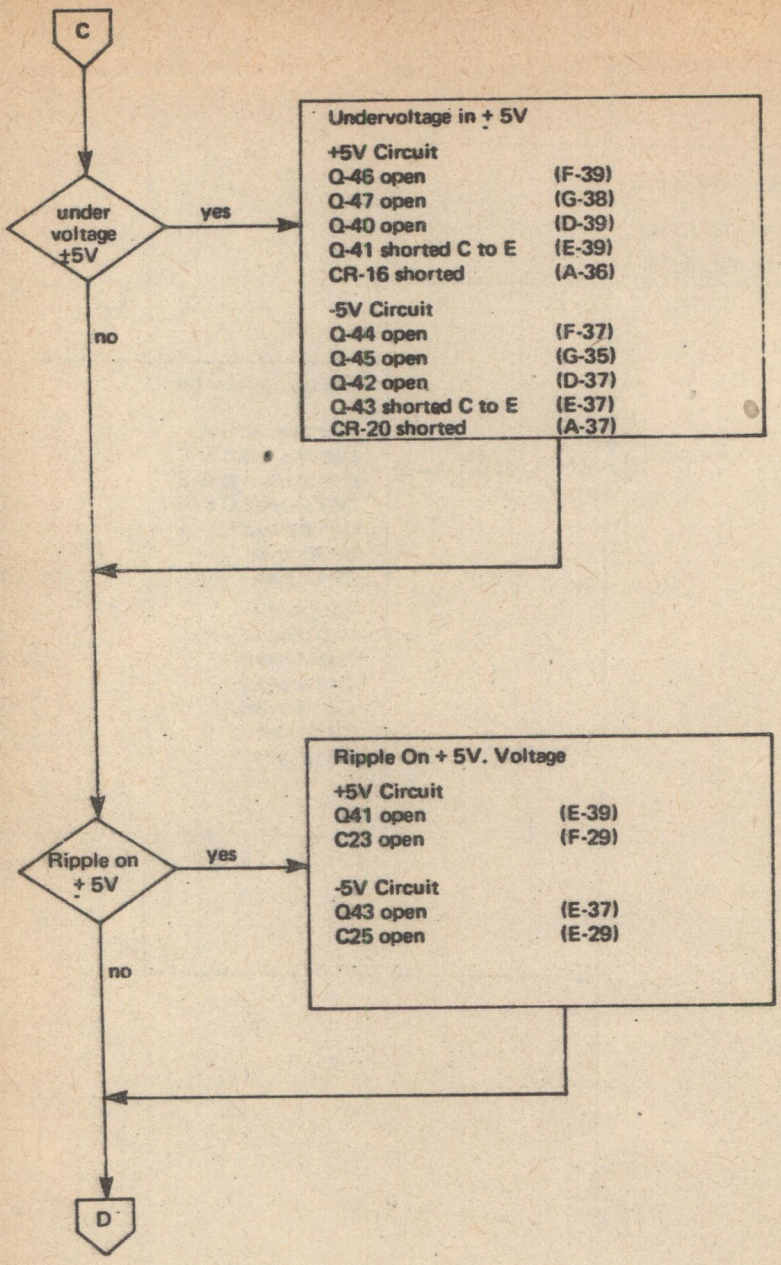
Designation	Card Description
A1	Write Head Cable
A2	Transport Harness
A3	Control Panel Cable
A4	
A5	
A6	Transport Interface
A7	Terminator
A8	Transport I/O Cable
A9	
A10	Parity Generator/ Check
A11	Read Strobe
A12	Terminator
A13	Read/Write I/O Cable
A14	Read Amp Output
A15	

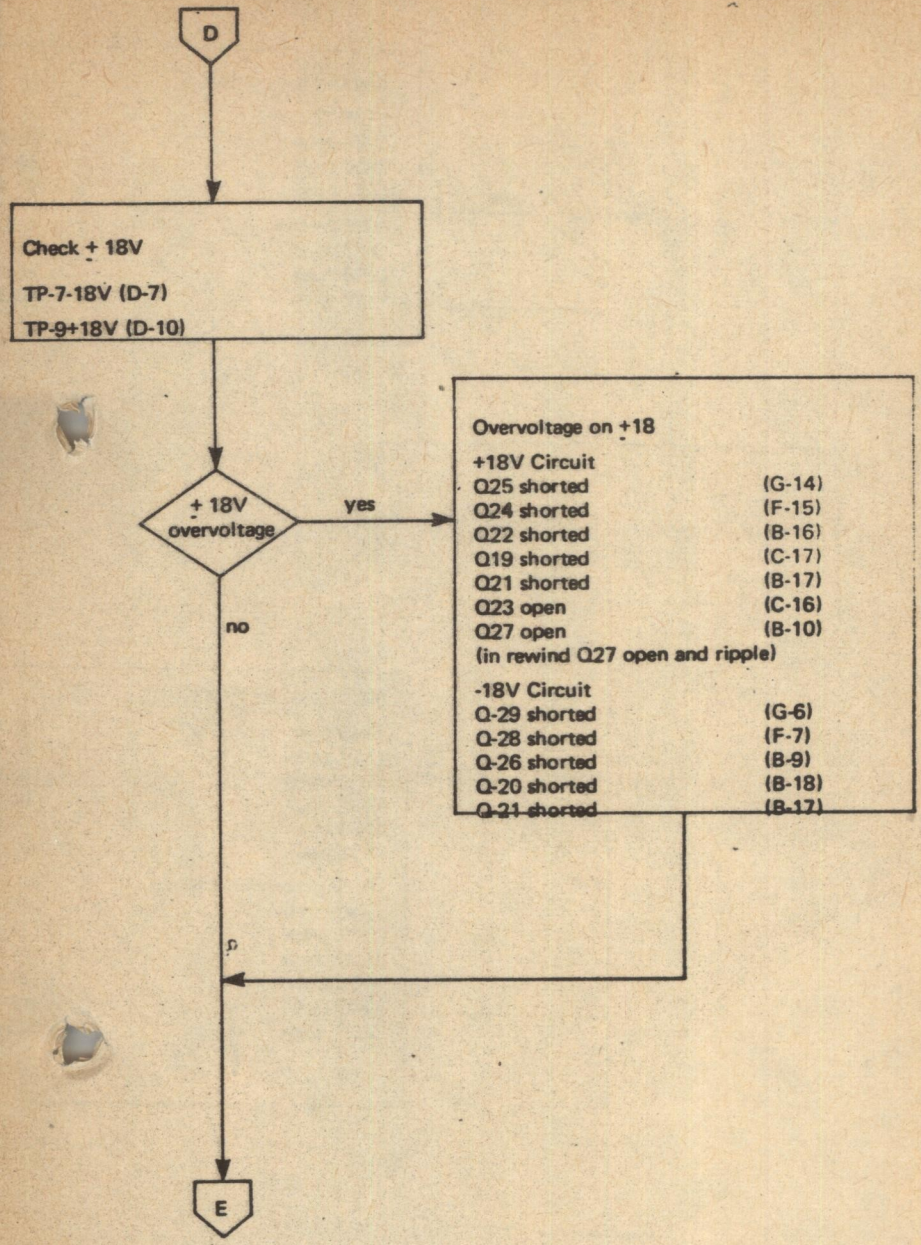
Designation	Card Description
A16	Read Head Cable
B1	Dual Reel Servo
B3	Capstan Amplifier
B5	Regulator
B6	Transport Control
B7	Ramp Generator/ Sense Amplifier
B8	Write Amplifier
B9	Write Amplifier
B10	Write Amplifier
B11	CRC Generator
B12	Amplifier Interface
B13	Write Control
B14	Read Amplifier
B15	Read Amplifier
B16	Read Amplifier

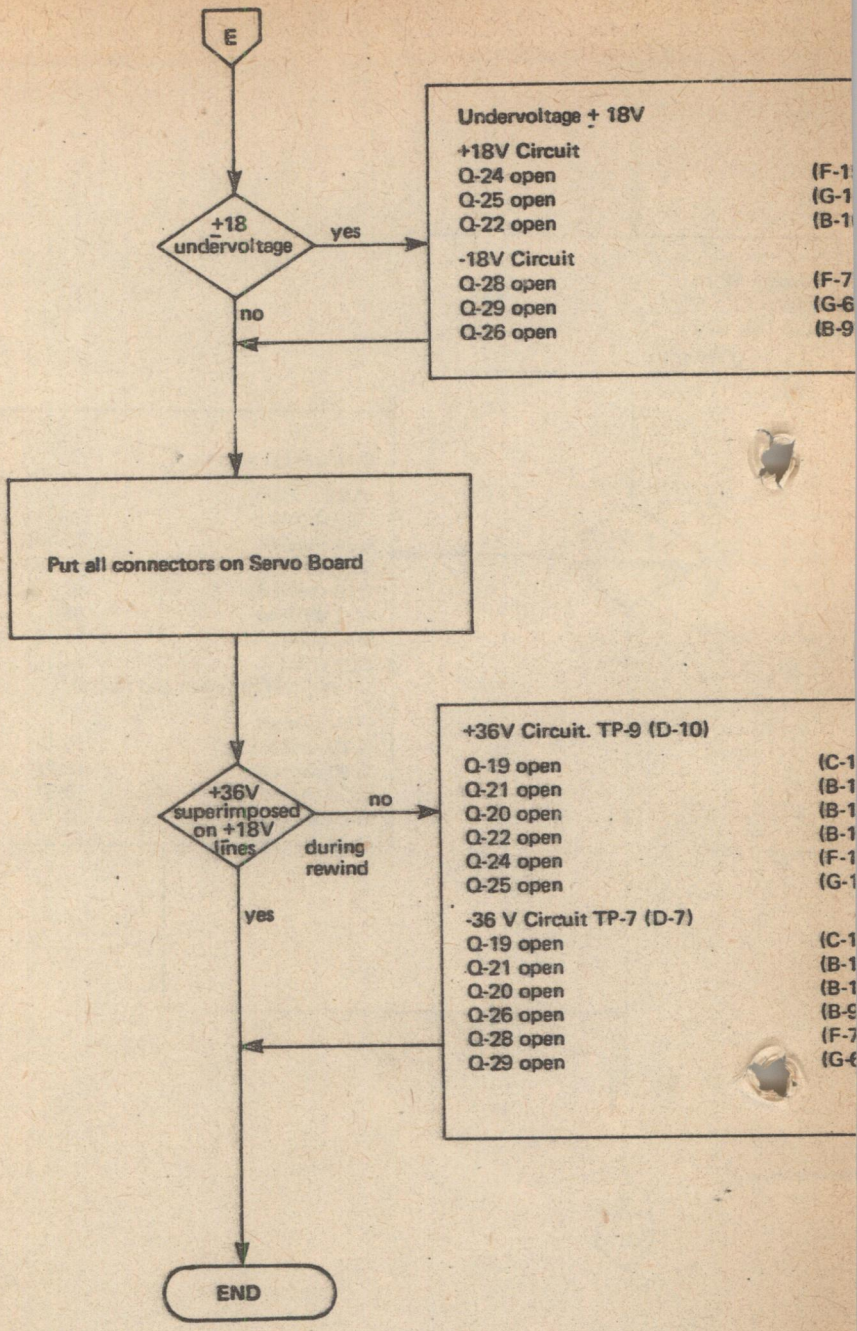

Entry to Servo Power Supply Troubleshooting
Remove all connectors from Servo Board except J-15 (B-38) and J-16 (E-18)
Fuse Blowing
yes
Check all power transistors for shorts, usually Base to Collector (G-1, to 39)
no
Check ± 10V
TP 12 +10V (D–28)
TP 13 -10V (C-28)
+10V over voltage
yes
+10V Circuit
Q-48 shorted C to E (D-33)
Q-54 shorted C to E (F-33)
Q-55 shorted C to E (G-25)
Q-49 open (E-33)
CR-16 open (A-36)
CR-17 open (A-37)
-10V Circuit
Q-50 shorted C to E (E-35)
Q-52 shorted C to E (F-35)
Q-53 shorted C to E (G-30)
Q-51 open (E-35)
CR-19 open (A-37)
no
A

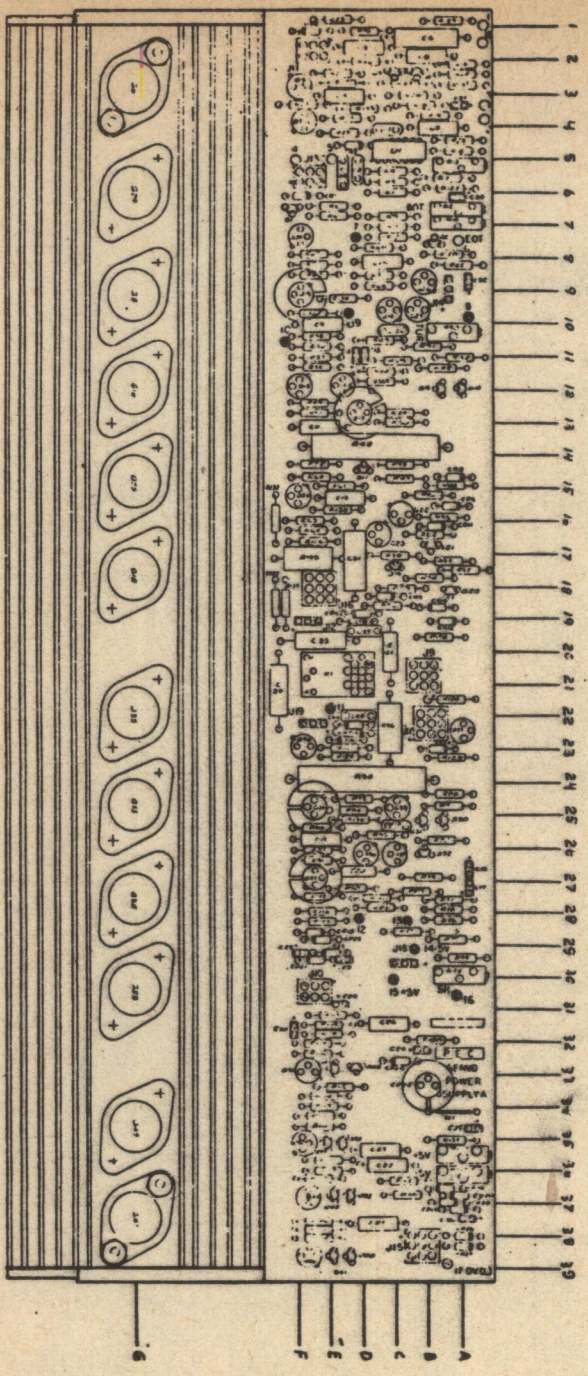

A
+10V undervolt age
yes
no
+10V Circuit
Q48 open (D-33)
Q49 shorted (E-33)
Q54 open (F-33)
Q55 open (G-25)
CR-16 open (A-36)
-10V Circuit
Q-50 open (E-35)
Q-51 shorted (E-35)
Q-52 open (F-35)
Q-53 open (G-30)
CR-20 shorted (A-37)
Ripple on +10V
yes
no
if bias on Q48 (Q50) is just right ripple can be caused by
+10V Circuit
Q-49 open (E-33)
-10V Circuit
Q-51 open (E-35)
B

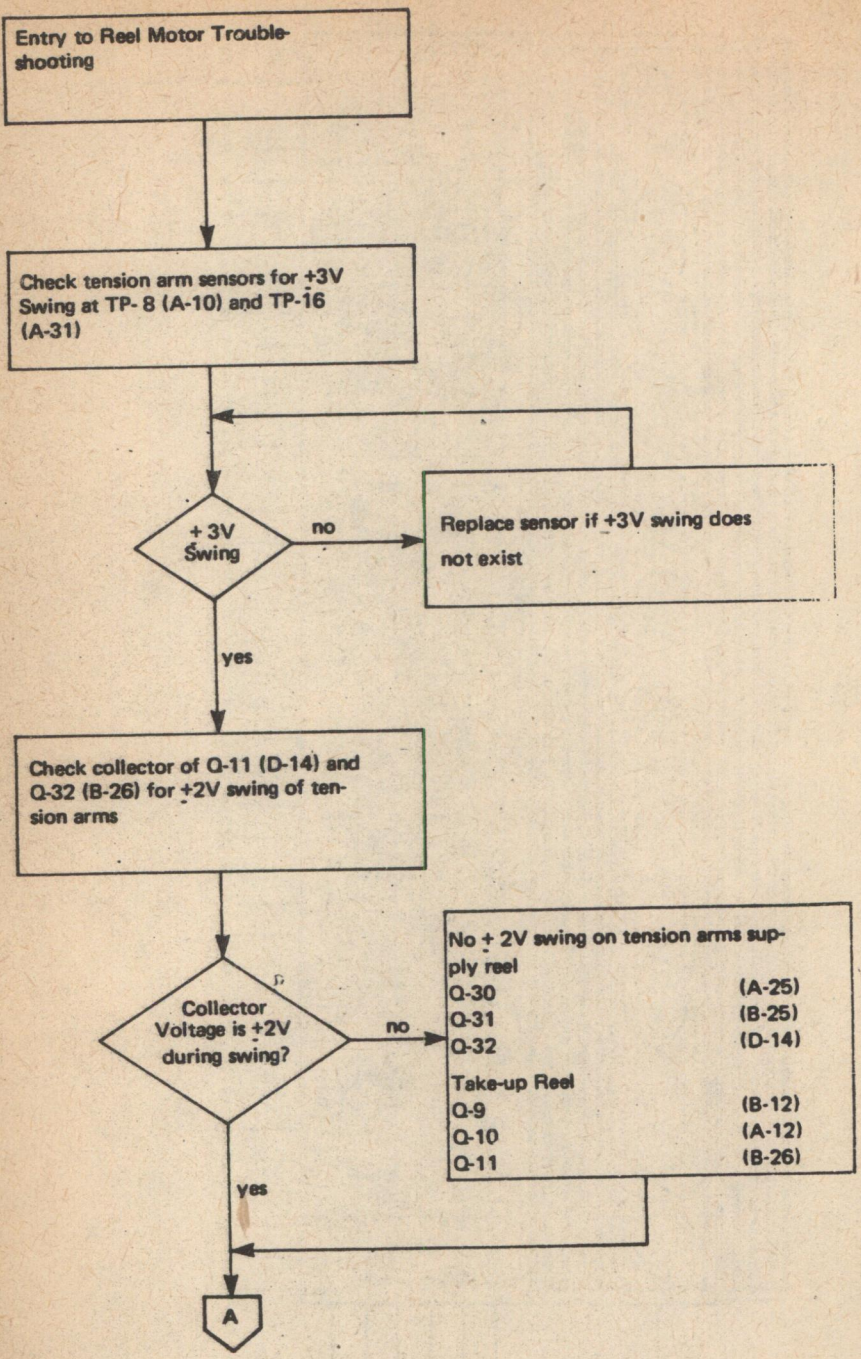

B
Check + 5V Circuit
TP 15 +5V (C-30)
TP 14 -5V (B-29)
+5V overvolt-age
yes
no
Overvoltage in + 5V
+5V Circuit
Q40 shorted C to E (D-39)
Q46 shorted C to E (F-39)
Q47 shorted C to E (G-38)
Q41 shorted C to E (E-39)
CR16 open (A-36)
CR17 open (A-37)
-5V Circuit
Q42 shorted (D-37)
Q44 shorted (F-37)
Q45 shorted (G-35)
Q43 shorted (E-37)
CR20 open (A-37)
CR19 open (A-37)
C

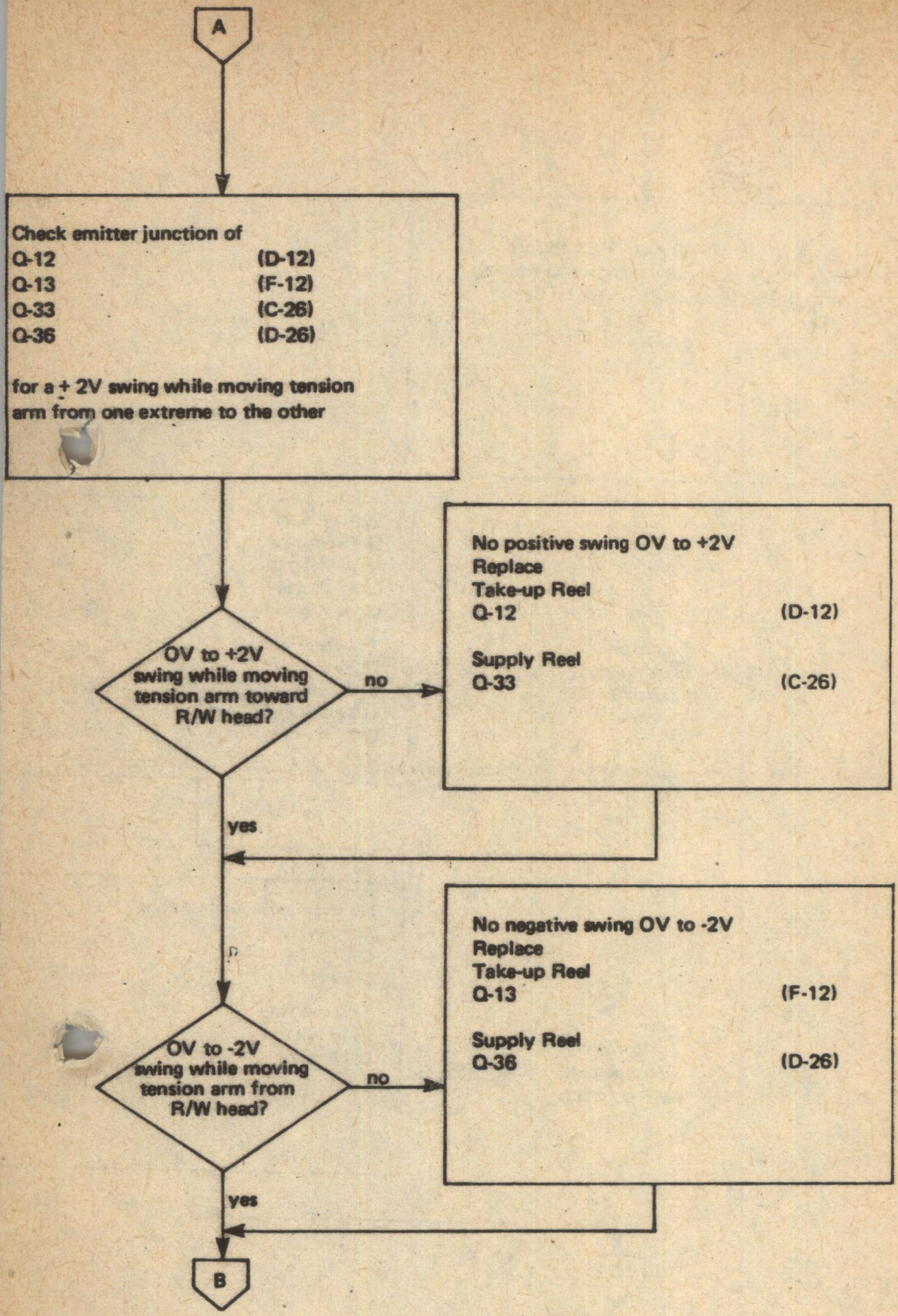

C
under voltage ±5V
yes
no
Undervoltage in ± 5V
+5V Circuit
Q-46 open (F-39)
Q-47 open (G-38)
Q-40 open (D-39)
Q-41 shorted C to E (E-39)
CR-16 shorted (A-36)
-5V Circuit
Q-44 open (F-37)
Q-45 open (G-35)
Q-42 open (D-37)
Q-43 shorted C to E (E-37)
CR-20 shorted (A-37)
Ripple on ± 5V
yes
no
Ripple On ± 5V. Voltage
+5V Circuit
Q41 open (E-39)
C23 open (F-29)
-5V Circuit
Q43 open (E-37)
C25 open (E-29)
D

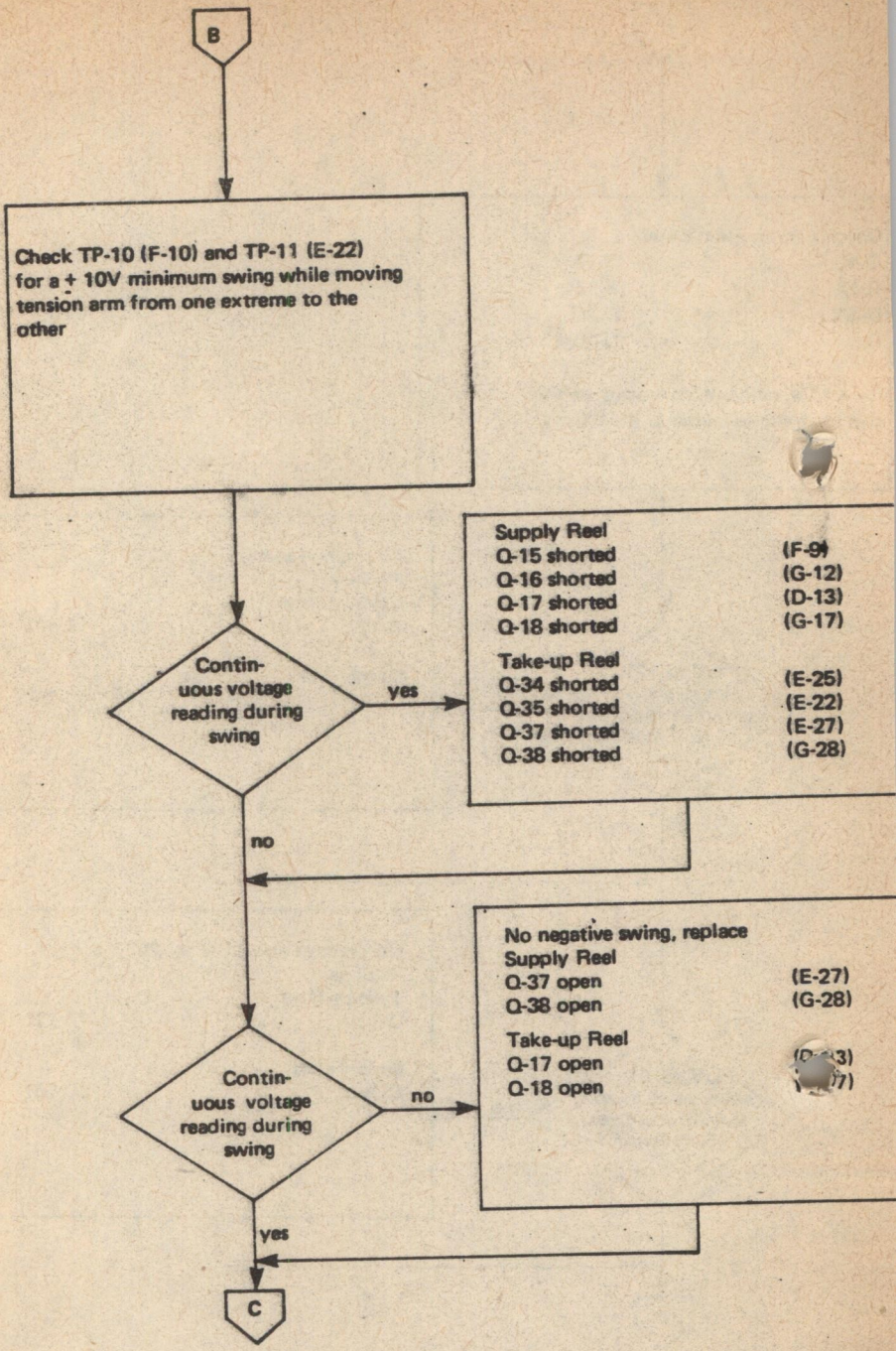

D
Check ± 18V
TP-7-18V (D-7)
TP-9+18V (D-10)
± 18V overvoltage
yes
no
Overvoltage on ±18
+18V Circuit
Q25 shorted (G-14)
Q24 shorted (F-15)
Q22 shorted (B-16)
Q19 shorted (C-17)
Q21 shorted (B-17)
Q23 open (C-16)
Q27 open (B-10)
(in rewind Q27 open and ripple)
-18V Circuit
Q-29 shorted (G-6)
Q-28 shorted (F-7)
Q-26 shorted (B-9)
Q-20 shorted (B-18)
Q-21 shorted (B-17)
E

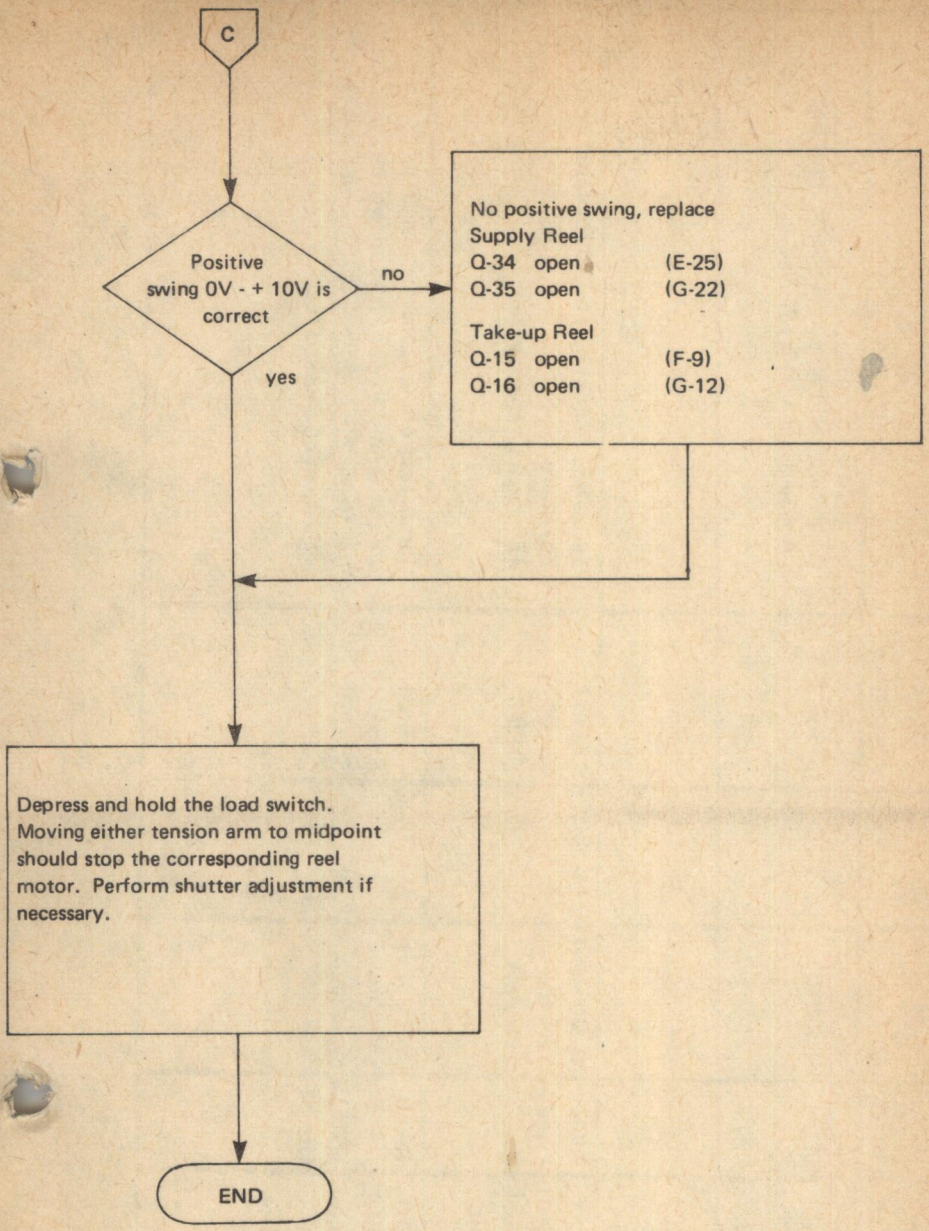

E
±18 undervoltage
yes
no
Undervoltage ± 18V
+18V Circuit
Q-24 open
Q-25 open
Q-22 open
-18V Circuit
Q-28 open
Q-29 open
Q-26 open
Put all connectors on Servo Board
+36V superimposed on +18V lines
no
during rewind
yes
+36V Circuit. TP-9 (D-10)
Q-19 open
Q-21 open
Q-20 open
Q-22 open
Q-24 open
Q-25 open
-36 V Circuit TP-7 (D-7)
Q-19 open
Q-21 open
Q-20 open
Q-26 open
Q-28 open
Q-29 open
END




Entry to Reel Motor Trouble-shooting
Check tension arm sensors for ±3V Swing at TP- 8 (A-10) and TP-16 (A-31)
+ 3V Swing
no
Replace sensor if +3V swing does not exist
yes
Check collector of Q-11 (D-14) and Q-32 (B-26) for ±2V swing of tension arms
Collector Voltage is ±2V during swing?
no
No ± 2V swing on tension arms supply reel
Q-30 (A-25)
Q-31 (B-25)
Q-32 (D-14)
Take-up Reel
Q-9 (B-12)
Q-10 (A-12)
Q-11 (B-26)
yes
A


A
Check emitter junction of
Q-12 (D-12)
Q-13 (F-12)
Q-33 (C-26)
Q-36 (D-26)
for a ± 2V swing while moving tension arm from one extreme to the other
OV to +2V swing while moving tension arm toward R/W head?
no
No positive swing OV to +2V
Replace
Take-up Reel
Q-12 (D-12)
Supply Reel
Q-33 (C-26)
yes
OV to -2V swing while moving tension arm from R/W head?
no
No negative swing OV to -2V
Replace
Take-up Reel
Q-13 (F-12)
Supply Reel
Q-36 (D-26)
yes
B


B
Check TP-10 (F-10) and TP-11 (E-22) for a ± 10V minimum swing while moving tension arm from one extreme to the other
Contin-uous voltage reading during swing
yes
Supply Reel
Q-15 shorted (F-9)
Q-16 shorted (G-12)
Q-17 shorted (D-13)
Q-18 shorted (G-17)
Take-up Reel
Q-34 shorted (E-25)
Q-35 shorted (E-22)
Q-37 shorted (E-27)
Q-38 shorted (G-28)
no
Contin-uous voltage reading during swing
no
No negative swing, replace
Supply Reel
Q-37 open (E-27)
Q-38 open (G-28)
Take-up Reel
Q-17 open
Q-18 open
yes
C


C
Positive swing 0V - + 10V is correct
no
yes
No positive swing, replace
Supply Reel
Q-34 open (E-25)
Q-35 open (G-22)
Take-up Reel
Q-15 open (F-9)
Q-16 open (G-12)
Depress and hold the load switch. Moving either tension arm to midpoint should stop the corresponding reel motor. Perform shutter adjustment if necessary.
END

Check all adjustments in order whenever any major assembly is replaced per page 6-23.

PROC	TEST EQ	TEST POINTS	ADJ	VALUE	LIMITS	ASSEMBLY	REMARKS
6.6.2.3.	DVM	+5/GND near J2 at rear of top most inst. read or write board	R4 on power supply	+5.0VDC	± .1VDC	101336 P.S.	Fixed and tracking oscillators also must be checked when +5V is adjusted.
6.6.3.3.	SCOPE	TP4,Ch1 TP1,GND piggyback at front left.	R5 on Fixed Osc.	(f=240 KHz) t=4.14μs cycle time	±.5%	P.E. Wr/ Contr. 101368	1μs pulses 4.14μs apart on 25IPS units. See figure 1. +5V must be checked first.
6.6.5.3.	SCOPE	TP4,Ch1 TP1,GND piggyback at rear left.	R5 on Tracking Osc.	(f=980 KHz) t=1.02μs cycle time		PE Read Recovery 101381	Install read board at top for ease of adj. Formatter must not be reading/writing. See figure 2. +5V must be checked first.

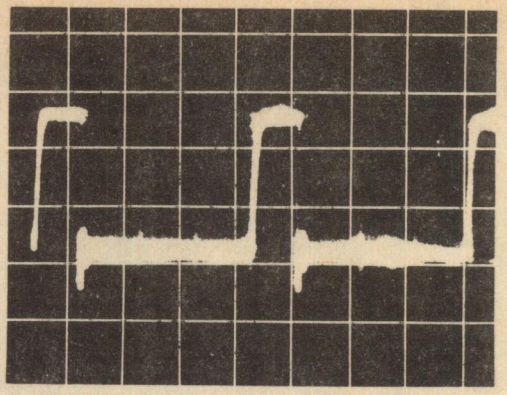


Figure 1
Scope was set at 1 us per Div.
.2V per Div. with a 10 to 1 Probe.

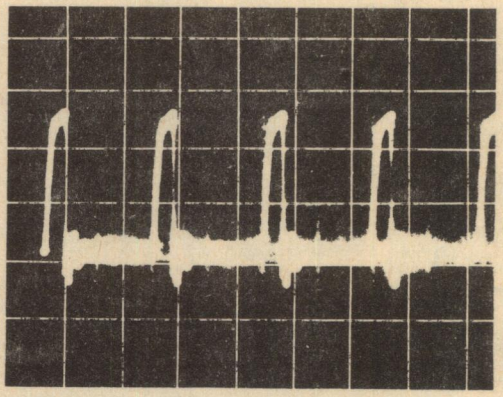


Figure 2
Scope was set at .5 us per Div.
.2V per Div. with a 10 to 1 Probe.

PERTEC 6640 TAPE TRANSPORT

Procedure assumes preventive maintenance and any adjustments related to parts replacement have been done per table 2. +5V and -5V Regulators must be checked prior to any electrical adjustment. Only the lower 3 digits of assembly number are referenced.

PROC	TEST EQ	TEST POINTS	ADJ	VALUE	LIMITS	ASSEMBLY	REMARKS
	DVM	TP9	NONE	+18V, FWD /REV MOTION		021 S&PS A	Servo and Power Supply A Checks
				+36 V, REWIND			
		TP 12 TP 13		+10v -10v			
		TP 14 TP 15	PROC 9-13	-5v +5v	COURSE CHECK		
		TP 17		GND			
9-13	DVM	TP 18 TP 19 TP 17	R 102 R 103 on S&PS A	+5VDC -5VDC GND	±.15V	241 C1 021 S&PS A	+5V and -5V Regulators Tape mounted at load point. Monitor between TP18(+5V) or TP19(-5V) on C1 board and TP 17 on S&PS A board. Adjust R 102(+5V) and R 103 (-5V) until both are within limits and within 0.07V (numerically) of each other. If adjustment is needed, Ramp Timing (Proc 50-54) and Tape Speed (Proc 60-63) MUST also be checked.
				Numerical Difference	<.07V		

+5V and -5V must be correct before adjustments are tried.

PROC	TEST EQ	TEST POINTS	ADJ	VALUE	LIMITS	ASSEMBLY	REMARKS
25-29	DVM	TP2 BOT TP1 EOT TP17	R9 R3 R2 & R10 MUST be fully clock-wise	+4.0V OFF TAB GND Difference	±.2V ≤.1V ≤+2.8V on TAB	949 EOT/BOT 021 S&PS A	EOT/BOT Amplifier Mount a tape with EOT/BOT mounted 1 foot apart. Perform at room temp. Located on 2-4" PCB mounted on Write Lockout bracket at rear of tape deck. Monitor between TP2 (off BOT) or TP1 (off EOT) on EOT/BOT Amplifier and TP17 (Gnd) on Servo and P.S.A. Adjust R9 (off BOT) and R3 (off EOT) until both are within limits and within .1V (numerically) of each other. TP2 (on BOT) and TP1 (on EOT) should read 2.8V maximum on tab.
30-34 35-39	DVM	TP4 BOT TP6 EOT TP17	R2 R10	+.85V onBOT ≥+3.0V off BOT +.2V ON EOT ≥+2,8V off EOT GND	≤ .9V ≤ .3V	021 S&PS A	BOT Amplifier and EOT Amplifier For those drives without additional EOT/BOT Amplifier PCBA.
60-63	Observe	Outer strobe	R29 None		≤1% Forward ≤3% Reverse	241 C1	Tape Speed. Move tape forward manually and adjust R29 on Tape Control (C1) Board until outer pattern (for 60 cps drives) on strobe disc. on capstan appears stationary.

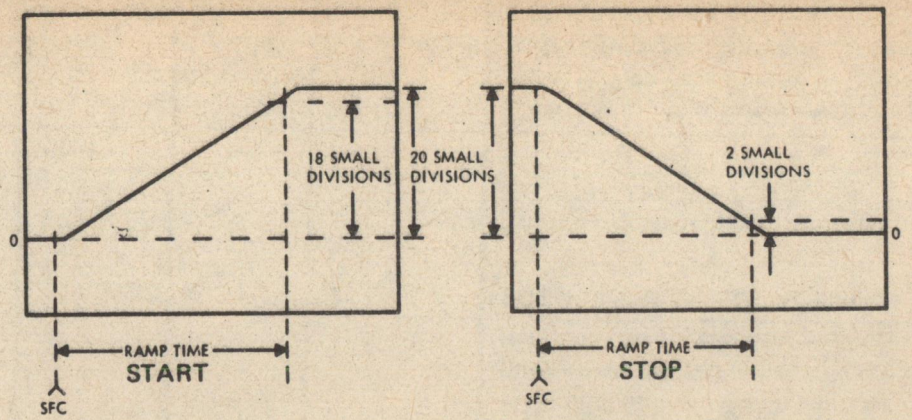


Figure 3. Ramp Levels and Timing

Measure from 0 to 90%

Table 1

Multi-purpose program for mag. tape alignment.

Start/stop Ramp: Forward, set AC0 = 50 and AC1 = 7777; Reverse, change AC0 = 40. (1 ch. block)

Write all 1's: Continuous, loc. 10 = 773; Records, loc. 10 = 771. Exam 0, Data switches = 177777, Continue. For alternate data change the data switches to 141075 (Track 4 = 1 if AC0 = 150).

XX = 20, 9ch/1600
22, 9ch/ 800
= 23, 7ch

AC0 = 50, WR odd
150, even
40, backspace
00, READ

AC1 = 7777, RAMP
7700, 100 char.
4000, max char.

AC2 = 11, starting address

0/062677 IORST
1/0635XX SKPBZ
2/000777 JMP. – 1
3/074477 READS 3
4/054011 STA 3
5/0611XX DOAS 0, MTA
6/0720XX DOB 2, MTA
7/0670XX DOC 1, MTA
10/000773 Continuous
or 771 Records
11/manual
–/pattern

For 1 char read, locs 6 & 7 may be changed to 0706XX, DIB 3; and 0664XX, DIC 1.

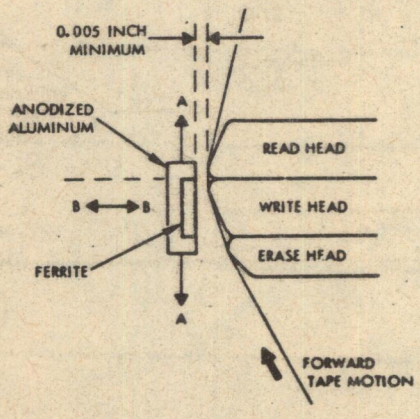
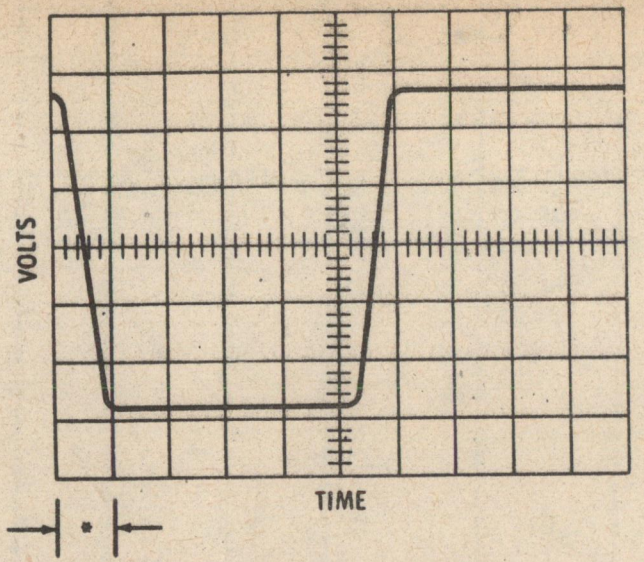


Figure 4. Flux Gate Adjustment

+5V and –5V regulators must be correct before adjustments are tried.

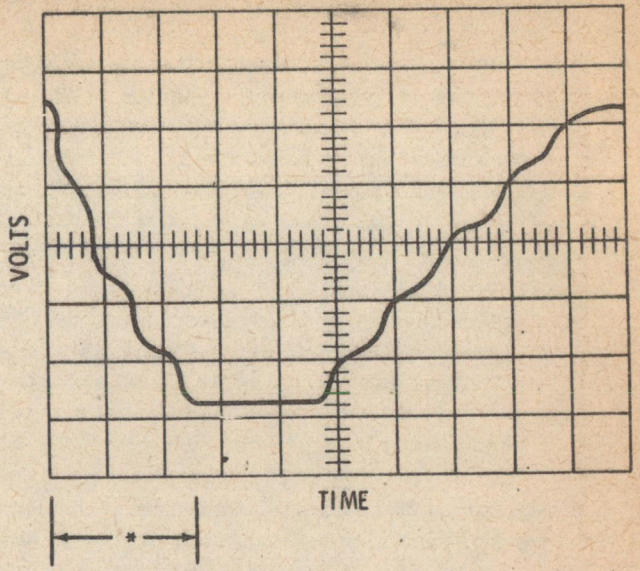
PROC	TEST EQ	TEST POINTS	ADJ	VALUE	LIMITS	ASSEMBLY	REMARKS
50-54	SCOPE	TP 5 TP 17	R915	12.2 MS for 90% of forward slope GND	±.6 ms	241-C1 021 S&PSA	Ramp Timing: (Start/Stop Time) Trig: CH 1, +, 2MS/Div, AC Coupled. Use program in Table 1, writing 1 ch. blocks. Adjust variable vertical gain for presentation 4 large divisions high. Observe slope at 18 small divisions from start of slope. (see Figure 3.) To check in reverse, change AC0 to 000040.
69-73	SCOPE	TP 104 to TP 904 TP 17	R117 to R917	6.2V P-P GND	±.3V PP	346 Data F 021 S&PSA	Read Amplifier Gain: Trig: INT. AC Couple CH1, 2V/Div. Tape Speed must be correct before checking gain. Write all 1's using program in Table 1. Rewind. Manually move tape forward and adjust R117 to R917 for 6.2V peak to peak on Test-Points TP104 to TP904; Use Standard Level Output Tape if available or a good quality scratch tape.
74		TP 6 TP 17, GND	None	+8.4v Write Mode +2.4V Read Mode IRTH2 False +1.2V, Read IRTH2 True	±.25V	346 Data F 021 S&PSA	Threshold Generator Check: If limits are exceeded a fault exists in the threshold circuitry.

PROC	TEST EQ	TEST POINTS	ADJ	VALUE	LIMITS	ASSEMBLY	REMARKS
96	SCOPE	TP 104 to 904	Flux gate	Crosstalk	≤1V P-P	346 Data F	Flux Gate Adjustment (Crosstalk) Trig Internal. Observe with Ch 1. Load scratch tape and move slightly reverse from load point. Holding fixed reel manually remove tape from capstan and carefully take up slack tape. While writing all 1's with the program in table 1, observe TP104 through TP904. Waveforms should be sinusoidal with no pronounced peaks, and crosstalk less than 1 V p-p. If not, stop the tape (reset) and loosen, slightly, the two small phillips screws holding the flux gate from the rear side of the tape deck. These will allow adjustment in direction A of Figure 4. Insert a piece of tab card between the gate and head. Holding the flux gate gently against the head, adjust the small allen screw on the gate to just contact the limit stop, and barely snug the two screws at the rear. Mount tape and reinitiate the program. While observing the crosstalk on TP604 and TP704 simultaneously, nudge the gate mount in direction(s) A for minimum crosstalk and tighten the phillips screws. Recheck all tracks and verify the ≤.005 clearance.
		CH1,TP604 CH2,TP704			≤.005" clearance from inner and outer tracks		
		TP 17		GND		021 S&PSA	



* FALL TIME MUST BE LESS THAN ONE DIVISION

Figure 5 . Skew Waveform (Good)



* FALL TIME EXCEEDS ONE DIVISION

Figure 6 Skew Waveform (Poor)

NOTE: Leave scope settings established in Proc 91 intact for use in proc 93.

PROC	TEST EQ	TEST POINTS	ADJ	VALUE	LIMITS	ASSEMBLY	REMARKS
90							Skew Measurement and Adjustment. The adjustments for +5V and -5V Regulators, Tape Speed, Read Amplifier Gain, and Flux Gate should all be correct before any attempt to adjust head skew. Requirements for PE read skew are not as critical, as for NRZI, because of PE channel buffers for read data recovery.
91	Scope	TP10	.0005" shims (max=4) may be added to or removed from ONE guide post base end (near deck) Each shim = 42μ inch.	MINIMUM. Fall time = from 5 to 95% of leading edge	<200μ inch (4 small divisions)	346 Data F	Write Skew. Power Down when changing connectors or PCBA's. Plug write head connector into read head (J2) receptacle and leave read cable unplugged. Trig – on CHI alternate; CHI = 1V/Div. Load an 800 CPI Master Alignment Tape and move tape forward. Adjust horizontal (time/div.) to display one complete cycle over 10 divisions; thus each small division = 50μ inch. Figures 5 and 6 show good and poor examples of wave form at TP 10.

PROC	TEST EQ	TEST POINTS	ADJ	VALUE	LIMITS	ASSEMBLY	REMARKS
92		TP 17	Careful not to lose spring and washer from guide	GND		021 S&PSA	If outside limits, ease the tape off a head guide cap toward the spring-loaded washer by 1 or 2 thousandths inch; first off the upper, then the lower guide, to see which movement improves the display. Remove shims from that guide where movement improved the waveform, if any; or add shims to the opposite guide post. Recheck. Power Down and replace write connector to J1, read connector to J2. Leave scope settings and probes intact for READ skew check proc. 93.
93	SCOPE	TP 10 TP 17	Check Readjust (proc 91 & 92) Wr Skew if outside limits	Fall time = from 5 to 95% of leading edge	<400μ inch (8 small divisions)	346 Data F 021 S&PSA	Read Skew. Trig — on Ch1, alt; Ch1 = 1V/Div. Same TP and Scope settings (approx) as proc 91. Display 1 full cycle; One small div = 50μ inch. Move tape forward on 800 cpi Master Alignment tape.

Table 2

Part Replacement Adjustments

Part Replaced	Auxiliary Adjustments	FE Ref/6640 Paragraph Reference	6 x 40 Manual Paragraph Reference
Control Switch	None	–	–
Photo-Tab Sensor	EOT/BOT Potentiometers on EOT/BOT Amplifier PCBA or Servo and Power PCBA	6-95	6.7.9
Tension Arm Sensor	Tension Arm Shutter	6-77, 6-81, or 6-85	6.7.2., 6.7.3, or 6.7.4.
Limit Switch Assembly	None	–	–
Capstan Drive Assembly	Tape Speed, Ramp on Tape Control PCBA	6-97	6.7.11
Reel Motors Assembly	Belt Tension	6-98	6.7.15
Power Supply Assembly	None	–	–
Tape Control PCBA	Ramp Timing and Tape Speed	6-50, 6-60	6.6.9, 6.6.10
Data PCBA	Read Amplifier Gain, Read Staticiser, Write Skew (6X40 Only)	6-69, 6-90	6.6.12 or 6.6.13, 6.6.15 or 6.6.16, 6.7.6.2.
EOT/BOT Amplifier Assembly	None	–	–
Head	Read Skew Adj., Write Skew Adj., (6X40 Only), Read Amplifier Gain	6-69 6-90	6.7.5, 6.7.6, 6.6.12 or 6.6.13
Write Lockout Assembly	None	–	–
Servo and Power Supply PCBA	+5v and -5v Regulators EOT/BOT Amplifiers, Reel Servo Gain, Rewind Speed (Servo and Power -B Only), Capstan Offset and Tension Arm	6-9, 6-14, or 6-19, 6-25, 6-30, 6-40, 6-45, 6-50, 6-55, 6-64	6.6.3, 6.6.4, 6.6.6, 6.6.7, 6.6.11

Table 4

System Troubleshooting

Symptom	Probable Cause	Remedy	Reference
Tape does not tension and the capstan shaft rotates freely when the LOAD control is depressed for the first time after	Interlock relay K1 does not close.	Check operation of relay. Replace if necessary.	Paragraph 5-6, 5-8 or 5-10
	LOAD control is not operative.	Check operation of control. Replace if necessary.	Paragraph 5-6. 5-8 or 5-10.
	Relay driver defective.	Check collector voltage of Q56 with LOAD control depressed. It should be less than +1 volt. If greater, isolate defective relay driver component and replace.	Paragraph 5-6, 5-8 or 5-10
Tape is tensioned when the LOAD control is depressed but tension is lost when control is released.	Relay latching contacts 9 and 10 do not make.	Check that voltage at J9-7 goes to +5 volts when LOAD control is depressed.	Paragraph 5-6, 5-8 or 5-10
	Limit switch is not operative.	Adjust as described in Paragraph 6-82, possibly replace limit switch assembly.	Paragraph 6-82
Tape unwinds or tension arm hits stop when the LOAD control is depressed for the first time.	Tape is improperly threaded.	Rethread tape (see Figure 3-1).	Paragraph 3-3
	+5 or -5 volts is missing from tension arm sensor.	Check tension arm sensor lamps. Isolate problem if lamp is extinguished.	Paragraph 6-83
	Fault in reel servo amplifier.	Check that movement of reels responds to tension arm position without tape on the transport.	Paragraph 5-7, 5-9 or 5-11

Symptom	Probable Cause	Remedy	Reference
Tape "runs away" or rewinds when LOAD control is depressed for the second time.	Fault on Tape Control or capstan motor assembly.	Replace or repair Tape Control PCBA or capstan motor assembly.	Paragraph 5-8 or Paragraph 6-105
Tape runs past the BOT marker.	BOT tab dirty or tarnished.	Replace tab or increase sensitivity of photosensor amplifier.	Paragraph 6-25, 6-30, 6-35, 6-40, or 6-103.
	Photosensor not properly adjusted.	Adjust photosensor amplifier.	Paragraph 6-25, 6-30, 6-35, or 6-40.
	Photosensor or amplifier defective.	Check for appropriate voltage levels in sensor systems with tab not over photosensor. Check appropriate voltage levels in sensor systems when tab is over photosensor.	Paragraph 6-25, 6-30, 6-35, 6-40, or 6-103.
	Logic fault (Load flip-flop does not reset).	Replace or repair Tape Control PCBA	Paragraph 5-12
Transport does not move in response to SYNCHRONOUS FORWARD or SYNCHRONOUS REVERSE Commands.	Interface cable fault or receiver fault.	Check levels at outputs and inputs of receivers on Tape Control PCBA. Replace or repair cable or Tape Control PCBA.	Paragraph 5-12
	Transport is not READY	Replace or repair Tape Control PCBA.	Paragraph 5-12
	Fault in ramp generator or capstan servo amplifier.	Check TP5 on Tape Control PCBA. Replace or repair Tape Control or Servo and Power PCBA.	Paragraph 5-6, 5-8, 5-10, or 5-12

Table 4

System Troubleshooting

Symptom	Probable Cause	Remedy	Reference
Transport responds to SYNCHRONOUS FORWARD command, but tape is not written.	Write current is not enabled.	Check presence of Write Enable ring on supply reel, WRT EN indicator should be lit. Check TP1 on Tape Control PCBA (should be +5v for writing). Replace Write Lockout assembly if faulty. Check that WRT PWR is +5v at TP8 and -5v at TP7 on Data PCBA.	Paragraph 5-3 and Paragraph 5-12
	Write status or MOTION signal to Data PCBA is not correct.	Check receiver on Tape Control PCBA for WRITE status and on Data PCBA for WRITE status.	Paragraph 5-3 and Paragraph 5-12
		Check Data PCBA for MOTION signal at TP1. Replace or repair Data PCBA or Tape Control PCBA if faulty.	Paragraph 5-3 and Paragraph 5-12
	WRITE DATA or WRITE DATA STROBE is not received correctly on Data PCBA from interface.	Check presence of the strobe at TP3 on Data PCBA. Replace or repair Data PCBA or interface cable if faulty.	Paragraph 5-3
	Head not plugged in correctly.	Check J2 and J3 on Data PCBA. Read head cable enters head near the take-up reel) uses J3.	—

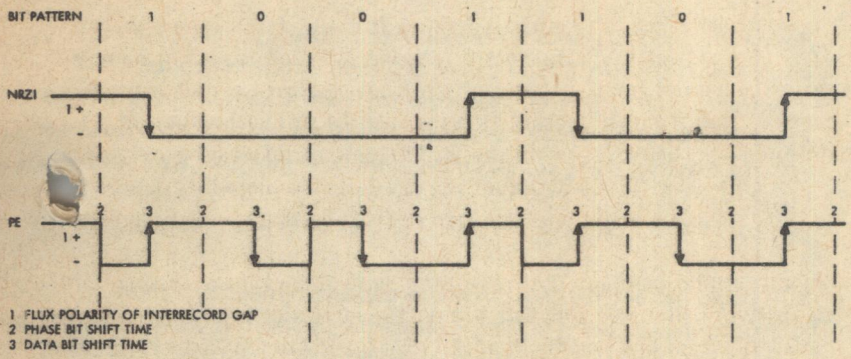
Table 4

System Troubleshooting (continued)

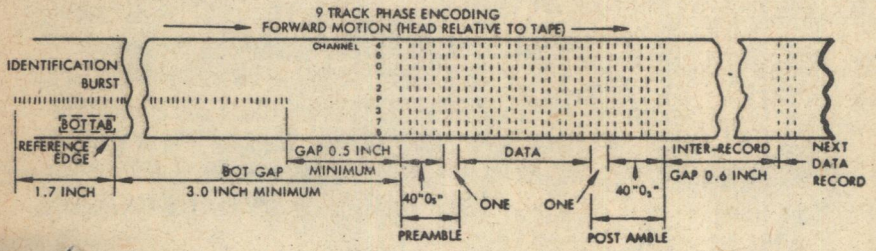
Symptom	Probable Cause	Remedy	Reference
Data are incorrectly written.	Incorrect data format.	Use correct format.	IBM Form A22-6589-3 (729 or 727 Series) IBM Form A22-6866-3 (2400 Series)
	Fault on 1 track due to failure in write circuits.	Check receiver and write amplifier on Data PCBA. Replace or repair Data PCBA if faulty.	Paragraph 5-3
	Intermittent WRT PWR, WRITE, MOTION, or WARS signal.	Examine those signals and replace or repair Tape Control PCBA or Write Lockout assembly.	Paragraph 5-3 and Paragraph 5-12
Correct tape cannot be read.	Interface cable or transmitter fault.	Replace or repair interface cable or Data PCBA	Paragraph 5-3
	Head is not plugged in.	Check J2 on Data PCBA. Check J3 on Data PCBA.	—
	Head and guides need cleaning.	Clean head and guides.	Paragraph 6-4
	Tape cleaner needs emptying.	Remove tape cleaner and clean.	Paragraph 6-4
	Read amplifier gains are incorrectly adjusted.	Check and adjust amplifier gains.	Paragraph 6-69

System Troubleshooting (continued)

Symptom	Probable Cause	Remedy	Reference
Correct tape cannot be read (cont'd)	Faulty write amplifier causes current to be passed through head while reading.	Check write amplifier output test points and replace or repair Data PCBA if faulty.	Paragraph 5 - 3
	Component fault in read channel.	Check test points on Data PCBA. Replace or repair Data PCBA.	Paragraph 5 - 3
	Envelope detector delays not correct.	Check TP106 - TP906 on Data PCBA for correct on and off times. Replace or repair Data PCBA.	Paragraph 5 - 4
	Threshold level incorrect.	Check level at TP6 on Data PCBA. Replace or Repair Data PCBA.	Paragraph 6 - 74



Comparison of NRZI and PE Recording Modes



9-Track PE Allocation, Spacing and Format

TESLA COMPATIBLE TAPE CONTROLLER

DESCRIPTION

The Tesla compatible magnetic tape controller is a double density device capable of writing tape of 800 B.P.I. I.B.M. format or 556 B.P.I. Tesla format.

Tesla is the manufacturer of the mainframe decks of some Seecheck customers in Czechoslovakia. Some of these customers also use I.B.M. mainframes so it is necessary for some Seecheck systems to read and write I.B.M. format and Tesla format tapes. The effect of this is that Seecheck systems requiring Tesla compatibility must have modified tape controller boards such as the old 048-108-2 or the later 048-437-2. Systems also requiring I.B.M. compatibility must have the later board (048-437-2).

This board has a single pole double throw switch mounted on the strengthening bar near the D edge connector. When this switch is positioned towards the front of the machine the board is in I.B.M. mode and will read and write I.B.M. format ('normal') tapes, i.e. normal gaps, normal CRCC treatment and 800 B.P.I. When the switch is positioned towards the back of the machine the controller is in Tesla mode and will read and write tapes in Tesla format i.e., 556 B.P.I. no CRCC written or read, CRCC error condition disabled, the read head is not turned on until 6 inches after B.O.T., the first record does not start until 12 inches after B.O.T. (SIB for read and SIB for write are increased), and the erased length of tape for one 'Erase' command is increased to 12 inches. The method by which these alterations are achieved is best explained by the combination of the 'Gap Timing Chart' and the Tesla version of sheet 4 of the logic diagram for the 048-437 board. It may be noted that to achieve the times for 'SIB Write' and 'Erase' and extension 'WDI' has been added to the delay counter.

Observation in this area will reveal that 'SIN Read' and 'SIN Write' times are virtually indentical to those in I.B.M. mode giving the same inter record gap but the Tesla counts are smaller, this is because the main oscillator is running about 33% slower to get the lower data density. This alteration in the main oscillator frequency is achieved when the switch

takes the +5V off the pot R2 which is set to the normal cycle time of 12.5 micro-seconds and supplies +5V to the new pot RA between F8 and H7 which is set for a cycle time of 18 micro-seconds. In Tesla mode the switch also applies +5V to a 1.5K resistor in parallel with R32 and R33 and so shortens the period of the monostable F8 from 175 micro-seconds to about 8 micro-seconds thus ensuring that the CRCC gate is opened and closed before anything can be read so that the LRCC (which is on tape where the CRCC would be in I.B.M. mode) is gated into the LRCC register.

The various devices attached to each end pin of the switch, which is connected to +5V by its centre pin, are isolated from the switch and thereby from each other by diodes which prevent the devices interfering with each other when that pin is not pulled high.

When no CRCC is used occasionally a record will have an LRCC of zero. When such a record is read it is essential that the software can detect the lack of LRCC.

To this end a JK flip-flop on D4 is cleared by CRCC gate ECCOO and then clocked by Transport Read Data Strobe. The $\overline{Q}$ output of this flop is put into bit 14 of the input status register. The result of this is that when there is no LRCC (i.e. the LRCC is zero), after the CRCC gate has cleared the flop no read strobe occurs so the $\overline{Q}$ output remains a logic high and a one appears in the status word in bit 14 informing the software of the lack of LRC character.

The software also needs to know when the board is in Tesla mode so the signal Tesla from J1 pin 2 is put into the input station register in bit 12. The polarity of these two bits has been chosen so that an ordinary board will look to the software like a Tesla compatible board in I.B.M. mode.

The diagnostic program needs to differentiate between the regular I.B.M. format tape controller and the dual density versions (Tesla or Aritma) even in I.B.M. mode, so bit 4 of the input status register which is normally the high density indicator bit and therefore strapped to a one and ignored on the 9/800 controller, is instead strapped to a zero. Bit 4 of the input status word from a board of device code 22 is now 'Single density controller'.

Testing this controller requires the updated version of TAPDA diagnostic program Rev.7. A listing of this program appears in the Seecheck Diagnostic Manual RDS–261–15. The diagnostic and acceptance program should be run with the board in I.B.M. mode and switch 12 down. Then the program should be restarted from 1,000 and the diagnostic and acceptance programs with the board in Aritma mode and switch 12 up.

GAP TIMING CHART TESLA/I.B.M./ARITMA

SIGNAL	TESLA		I.B.M.		ARITMA	
	Write Delay Count	Time in m.s.	W.D.Count	Time in m.s.	W.D.Count	Time in m.s.
S.I.B. Read	C.D.E.F.H.	541	C.D.E.F.	120	C.D.E.F.G.	337
S.I.N. or S.I.B. Erase and S.I.B. Write	C.D.H.I.	1140	C.D.H.	280	C.D.I.	772
S.I.N. Read and S.I.N. Backspace	D	23	C.D.	24	C.D.	35
S.I.N. Write	E	46	D.E.	48	E.F.	138
Main oscillator Cycle time	18 μ.s.		12.5 μ.s.		18 μ.s.	
One frame time	72 μ.s.		50 μ.s.		72 μ.s.	
Tape data density	556 B.P.I.		800 B.P.I.		556 B.P.I.	

ARITMA COMPATIBLE TAPE CONTROLLER

DESCRIPTION

The aritma compatible magnetic tape controller is a double density device capable of writing tape of 800 B.P.I. I.B.M. format or 556 B.P.I. Aritma format.

Aritma is the manufacturer of the mainframe decks of some Seecheck customers in Czechoslovakia. Some of these customers also use I.B.M. mainframes so it is necessary for some Seecheck systems to read and write I.B.M. format and Aritma format tapes. The effect of this is that Seecheck systems requiring Aritma compatibility must have modified tape controller boards such as the old 048-108-3 or the later 048-437-3. Systems also requiring I.B.M. compatibility must have the later board (048-437-3).

This board has a single pole double throw switch mounted on the strengthening bar near the D edge connector. When this switch is positioned towards the front of the machine the board is in I.B.M. mode and will read and write I.B.M. format ('normal') tapes, i.e. normal gaps, normal CRCC treatment and 800 B.P.I. When the switch is positioned towards the back of the machine the controller is in Aritma mode and will read and write tapes in Aritma format i.e., 556 B.P.I. no CRCC written or read, CRCC error condition disabled, the read head is not turned on until 3 inches after B.O.T., the first record does not start until 6 inches after B.O.T. (SIB for read and SIB for write are increased), and the erased length of tape for one 'Erase' command is increased to 6 inches. The method by which these alterations are achieved is best explained by the combination of the 'Gap Timing Chart' and the Aritma version of sheet 4 of the logic diagram for the 048-437 board. It may be noted that to achieve the times for 'SIB Write' and 'Erase' and extension 'WDI' has been added to the delay counter.

When in Aritma mode, to get the lower data density of 556 B.P.I. the main oscillator runs about 33% slower than I.B.M. mode. This alteration in the main oscillator frequency is achieved when the switch takes the +5V off the pot R2 which is set to the normal cycle time of 12.5 micro-seconds and supplied +5V to the new pot RA between F8 and H7 which is set for cycle time of 18 micro-seconds. In Aritma mode the switch also applies +5V to a 1.5K resistor in parallel with R32 and R33 and so shortens the period of the monostable F8 from 175 micro-seconds to about 8 micro-seconds thus ensuring that the CRCC gate is opened and closed before anything can be read so that the LRCC (which is on tape where the CRCC would be in I.B.M. mode) is gated into the LRCC register.

The various devices attached to each end pin of the switch, which is connect to +5V by its centre pin, are isolated from the switch and thereby from each other by diodes which prevent the devices interfering with each other when that pin is not pulled high.

When no CRCC is used occasionally a record will have an LRCC of zero. When such a record is read it is essential that the software can detect the lac of LRCC.

To this end a JK flop on D4 is cleared by CRCC gate ECCOO and then clocked by Transport Read Data Strobe. The $\overline{Q}$ output of this flop is put in bit 14 of the input status register. The result of this is that when there is no LRCC (i.e. the LRCC is zero), after the CRCC gate has cleared the flop no r strobe occurs so the $\overline{Q}$ output remains a logic high and a one appears in the status word in bit 14 informing the software of the lack of LRC character.

The software also needs to know when the board is in Aritma mode so bit 9 of the status word, which is normally the nine channel indicator and therefo strapped to a one and ignored by the software is instead connected to Aritn Bit 9 of the input status register from a device code 22 is now a low true Aritma indicator bit. The polarity of bits 9 and 14 have been chosen so tha an Aritma compatible board in I.B.M. mode will produce the same status w as an ordinary board.

The diagnostic program needs to differentiate between the regular I.B.M. fo tape controller and the dual density versions (Tesla or Aritma) even in I.B.M mode, so bit 14 of the input status register which is normally the high dens bit and therefore strapped to a one and ignored on the 9/800 controller, is instead strapped to a zero. Bit 4 of the input status word from a board of device code 22 is now 'Single Density Controller'.

Testing this controller requires the updated version of the diagnostic progra TAPDA Rev.7. A listing of this program appears in the Seecheck Diagnosti Manual RDS–261–15. The diagnostic and acceptance program should be r with the board in I.B.M. mode and switch 12 down. Then the program sho restarted from 1,000 and the diagnostic and acceptance programs with the board in Aritma mode and switch 12 up.

ENM PRINTER

ENM PRINTER

ENGLISH NUMBERING MACHINES

PRINTER – GENERAL DESCRIPTION

First read CENTRONICS GENERAL DESCRIPTION.

The ENM Printer differs from the Centronics in the following ways:–

It only uses a 5 x 7 dot matrix for normal character printing.

There is no priming circuit to clear the 132 character buffer so it does not insert a bit 8 in the first character, therefore it cannot detect a bit 8, consequently if more than 132 characters are loaded into this buffer the first ones drop out of the end (so to speak).

The software must decide when the buffer is full and sends a carriage return to initiate a print operation by engaging the clutch.

Another major difference is that the ENM timing fence produces only one pulse for a complete character, this starts a timing circuit which produces 6 pulses, one for the gap between characters and 5 for the 5 print operations of a character, which are fed to a ROM in a similar manner to the Centronics.

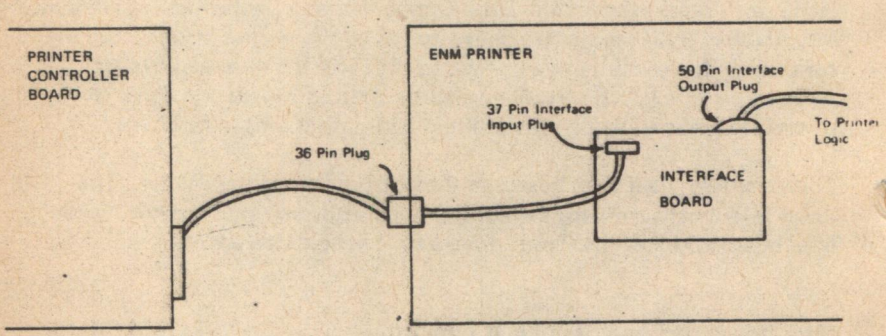
Because the input and output signals of an ENM Printer differ in detail to a Centronics Printer, an interface board has been fitted to the ENM Printer (RHS of Printer) to make the ENM compatible to a Centronics. It contains a 1 character 8 bit register which is strobed by the normal strobe from the controller. It also contains a one-shot to provide the 4 us acknowledge pulse we require. Also various invertors are fitted for correct signal levels to make it compatible. (A list of input and output pins is supplied).

There are two main logic boards at the bottom rear of the Printer. The lower level board contains the control logic, registers, etc., and the higher level board contains the Power drivers for solenoids, relays etc.

Information on Power supplies is supplied.

SIMPLIFIED SIGNAL FLOW FROM CONTROLLER TO OUTPUT OF ENM INTERFACE BOARD

CENTRONICS & ENM CONTROLLER TO PRINTER CABLE			INTERFACE BOARD (ENM)	
Signal	Controller Pin No.	Pin No. Printer End	Pin No. Input Plug	Pin No. Output Plug
$\overline{\text{ACKNOWLEDGE}}$	D6	10	10	11 ($\overline{\text{REQ DATA}}$)
BUSY	D7	11	11	13 ($\overline{\text{BUSY}}$)
DATA 7	D9	8	26	7 ($\overline{\text{DATA 7}}$)
DATA 6	D10	7	25	6 ($\overline{\text{DATA 6}}$)
DATA 5	D11	6	24	5 ($\overline{\text{DATA 5}}$)
DATA 4	D12	5	23	4 ($\overline{\text{DATA 4}}$)
DATA 3	D13	4	22	2 ($\overline{\text{DATA 3}}$)
DATA 2	D14	3	21	2 ($\overline{\text{DATA 2}}$)
DATA 1	D15	2	20	1 ($\overline{\text{DATA 1}}$)
$\overline{\text{STROBE DATA}}$	D22	1	36	9 (DATA STROBE)



OPERATION OF NEEDLE PRINTER

a). **START**

1. Plug into mains.

2. Press ON/OFF button – ON/OFF button lit up.

   2.1 If ON/LINE button lit up, drepress ON/LINE button and release – light will go out (now in local mode).

b). **CARRIAGE CONTROL TAPE: TO LOAD (Refer to Fig. 2)**

1. Open hinged cover.

2. Collect paper tape loop.

3. Lift SPROCKET WHEEL GUIDE.

   With SPROCKET HOLES nearer to the right of the paper tape, slip the paper tape loop between TAPE READ HEAD and TAPE READ BASE.

4. Make sure SPROCKET HOLES on the PAPER TAPE are fitted on the sprocket wheels.

5. Release SPROCKET WHEEL GUIDE and close hinged cover.

6. Depress TOP FORM button (refer fig.1) – paper tape moves to correct place.

c). **PAPER LOAD (Refer to Fig. 1)**

1. Open rear and front covers by depressing the TWO COVER RELEASE buttons, one either side of the printer, and open the covers, which are hinged to the front and back of the printer. (Do not lean on covers).

2. Move the PAPER RELEASE LEVER forward for loading.

3. If paper width different from paper used previously, depress RIGHT HAND TRACTOR LOCK and move tractor feed to appropriate position. Use FINE ADJUSTMENT KNOB to adjust paper.

4. Place paper in tray underneath printer.

5. Feed paper end through slot in bottom of printer upward to front of platen. Pull up enough paper for about a 12" length to show. (This is easier if the paper is folded to a point).

6. Lift TRACTOR CHAIN COVERS.

7. Place paper over tractor chain making sure the paper is placed correctly by checking that any horizontal lines are level.

8. Release TRACTOR CHAIN COVERS.

9. Replace the PAPER RELEASE LEVER to the back position.

10. Press in the RELEASE BUTTON (refer Fig.2) on the PAPER ADVANCE KNOB (refer Fig.2) and turn this knob to place the paper to 'Top of Form' by positioning the paper perforations just above the printer head (or as per separate operating instruction

11. Release the RELEASE BUTTON and ensure that the PAPER ADVANCE KNOB is locked by trying to turn it. If this knob still moves depress and release the release button again. Check that paper is correctly positioned.

12. Replace rear and front covers firmly.

d). PAPER THICKNESS AND PRINT TEST

1. Push PAPER THICKNESS CONTROL back.

2. Press PRINT TEST KNOB (on base of machine – refer Fig. 1).

3. If print is dark but not smudged, the printing is correct.

   Otherwise – move PAPER THICKNESS CONTROL forward and repeat 2 (above) until print is as stated in 3.

e). LIGHT AND HOOTER TEST

Push Lamp/Hooter button to the right on base of machine – (refer fig. 1) – the PAP OUT ON/LINE ON/OFF lamps should light and the hooter sound. Releasing the Lamp/Hooter button stops the test.

f). CHANGING THE RIBBON (OR TURNING IT OVER) – (Refer to Fi

The ribbon should be turned over every time a new set of paper is used (or as per separate operating instructions).

1. Switch off printer.

2. Open front cover (refer C.1).

3. For each RIBBON SPOOL in turn, move its locking lever towards front of machine. Lift spool off its SPINDLE.

4. Ease ribbon from the two BRASS GUIDES at either end of carriage.

5. Lift ribbon clear of PRINT HEAD and the two IDLERS.

6. Turn ribbon over i.e. interchange the SPOOLS (or put on new ribbon).

7. Fit ribbon spools back on spindles and lock into position. Allow ribbon to rest on carriage.

8. Fit ribbon into the two brass guides. Make sure ribbon is not twisted.

9. Fit ribbon behind head and in front of the two idlers. Make sure ribbon lies flat.

10. Turn one of the spindles gently to take up any slack ribbon.

11. Replace front cover firmly.

g). **END OF PAPER**

At the end of paper the hooter sounds. To stop hooter press the ON LINE button. The On Line button light will go out. The printer is now ready for a new set of paper to be loaded.

ENM POWER SUPPLIES

Board 1	+30v and 24v Power Transistors.
Board 2	+30v and 24v Regulation. + 5v Supplies.
Board 3	+12v and -12v Supplies.
Board 4	Mains Failure Detection.

TEST POINTS

Board 2	TP1	30V
	TP5	+24V
	TP2	+ 5V
Board 3	TP3	+12V
	TP4	-12V
Board 4	Ov picked up from top edge.	

h) TO CONNECT PRINTER TO ITS DRIVER

Once any or all of the following actions have been taken as appropriate:

A. Start
B. Load carriage control tape
C. Load paper
D. Paper thickness and print test
E. Lamp and Hooter test
F. Change ribbon

the printer is connected to its driver by pressing the ON LINE button which will light up.

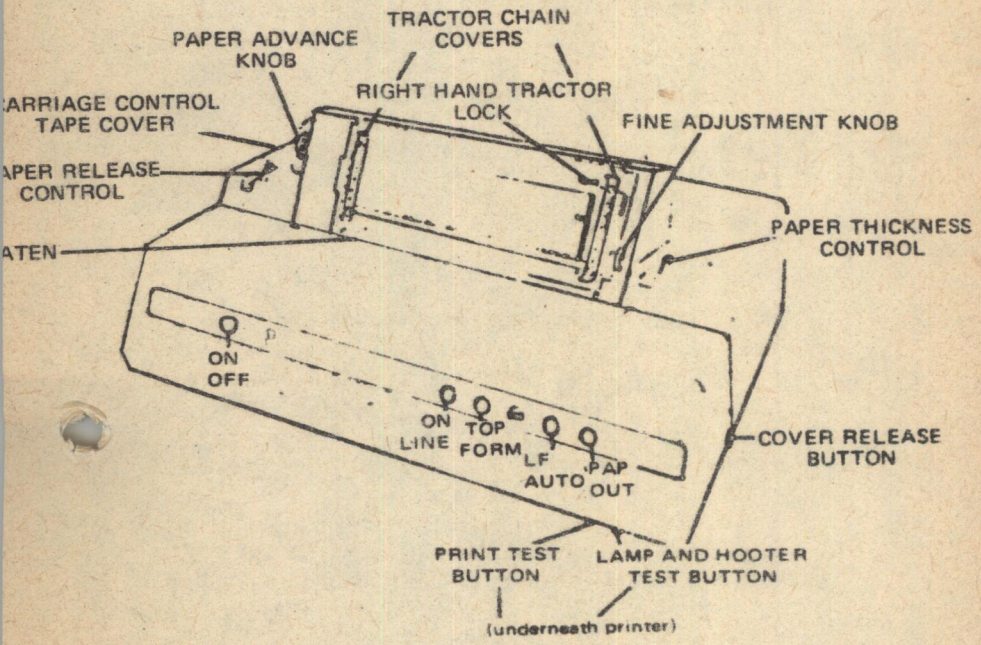


Figure 1. LABELLED DIAGRAM OF PRINTER

Figure 2. CARRIAGE CONTROL TAPE

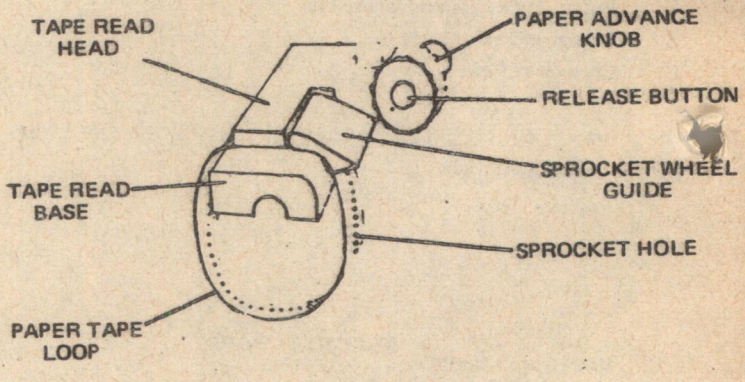
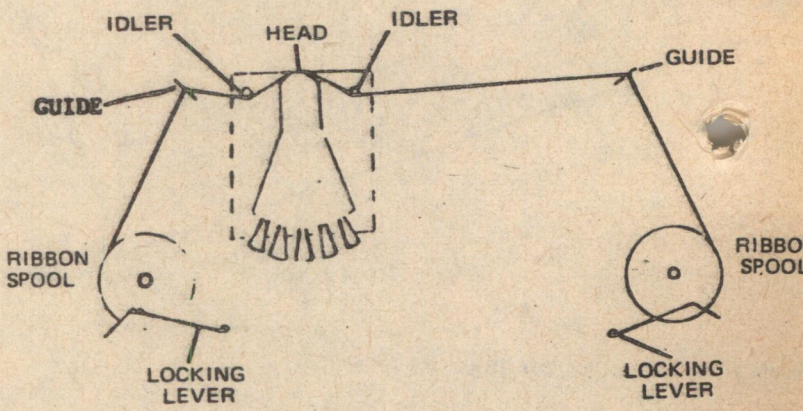
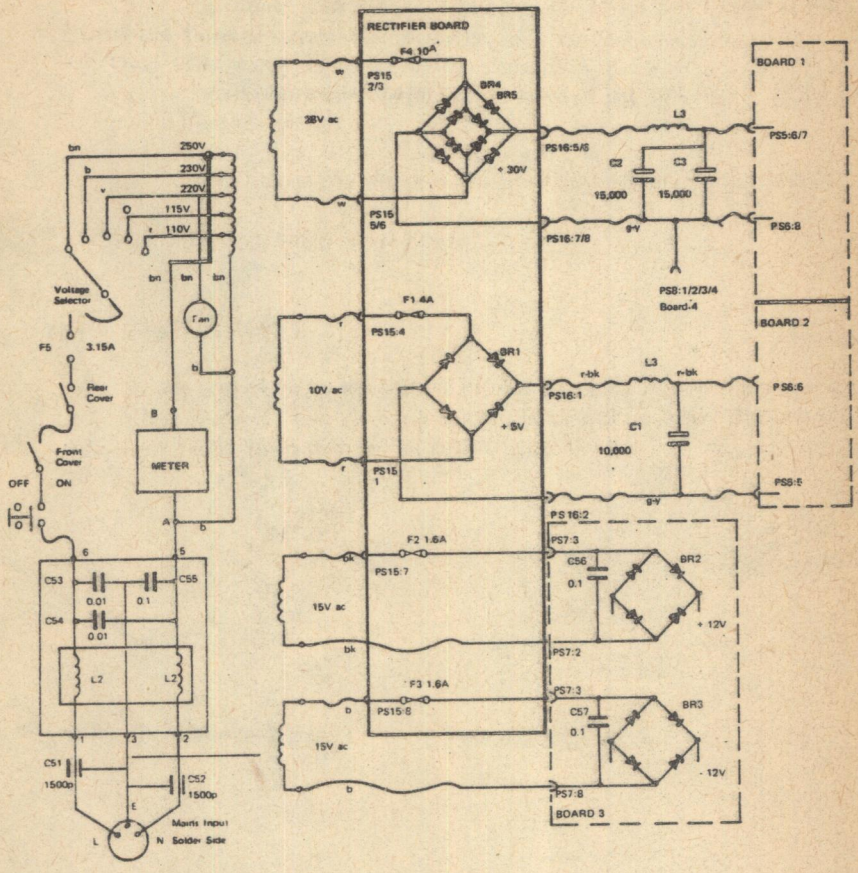


Figure 3. RIBBON PATH





POWER UNIT – MAINS INPUT

CENTRONICS 101A PRINTER

GENERAL DESCRIPTION

The Centronics Model 101A Printer is a medium speed impact printer, which uses a 9 x 7 dot matrix for character generation.

The seven print wires are held vertically in a jewel and print a character in 5 columns and 4 half columns as the head moves across the paper. The seven print wires are fired at the paper by seven solenoids.

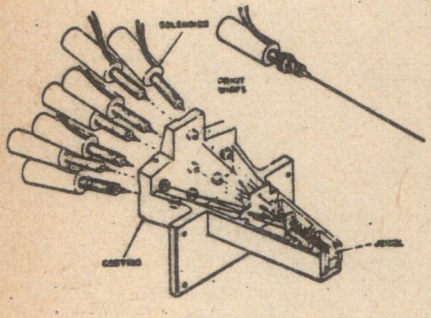


Figure 1-3. PRINT HEAD COMPONENTS

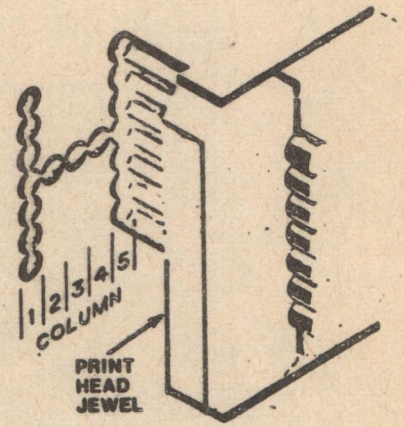


Figure 1-4. PRINTING THE LETTER (H)

The printer contains a 132 (8 bit) character input buffer memory shift register, which prints data at 165 characters per second.

Printing action is initiated automatically when this buffer is full or when a carriage return code has been received, the full or partially full buffer is then shifted out and printed.

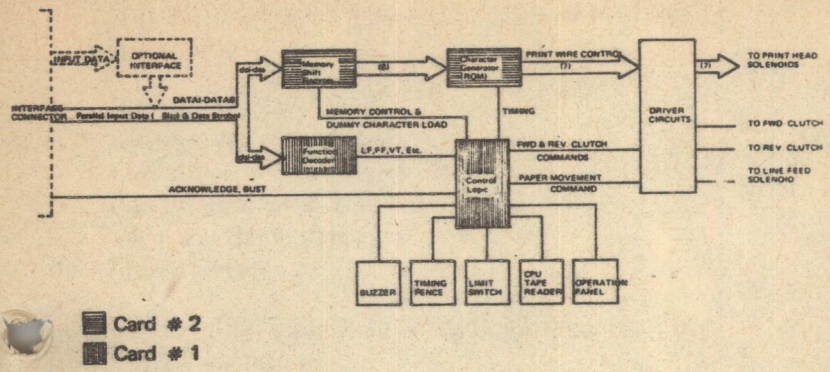
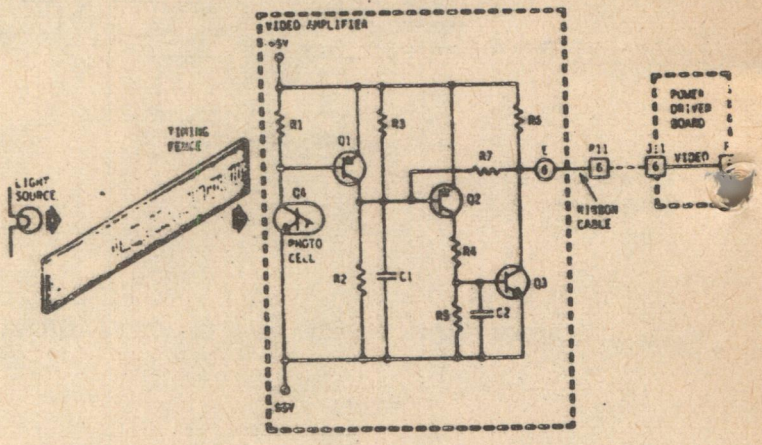


Figure 4–1. MODEL 101A FUNCTIONAL BLOCK DIAGRAM

When power is first switched on a priming circuit clears all F/F's and registers and puts a bit 8 in the first character of the 132 char buffer. As characters are fed from the computer via the Print Controller, a strobe, produced by the controller, strobes the data into the 132 character buffer. 7 us later the Printer sends back an acknowledge signal to the controller requesting more data. If a Carriage Return code is received it is decoded and allows the printer to clock (100KHz) the data through the buffer until bit 8 is detected and then engages the forward clutch driving the print head along the paper printing the characters. When the reverse clutch is engaged and the head is returning the prime operation is activated again placing a bit in bit 8 of the buffer for the next line.

If a special function is decoded, i.e. line feed, bell, form feed etc., it is decoded and not placed in the buffer, but sets a Busy F/F which prevents the acknowledge pulse being produced until the special function has been completed.



The buffer is clocked into the Read Only Memory (ROM) by a strobe which is produced from the timing fence. As the print head moves along its guide bar, a photo electric cell detects the change of light in the fence producing a 1ms pulse, the first of six such pulses strobe a character into the ROM, (this pulse is the gap between characters), the next five pulses are used to strobe full step ROM. There are also 4 half step pulses which feed the half step ROM, a total of 9 steps firing the solenoids to produce a character.

When bit 8 is detected at the output of the buffer (dummy character) it is "ANDed" with a magnetic switch that is made when the print head is at rest on the lefthand side of the carriage, this engages the forward clutch which moves the head across the paper and along the timing fence.

P.M. SCHEDULE FOR CENTRONICS PRINTERS

	Drawing Reference	
1.	HA–45	Oil gib for head bracket.
2.	HE–52	Clean timing fence with clean soft cloth. (MILD DETERGENT IF NEEDED. DO NOT USE ANY ALCOHOL –BASED CLEANING SOLUTION).
3.	HI–30	Grease on driving slide shaft ends at bushings HI–30.
4.	HH	Oil all shafts in form feed unit.
5.	HE–8 & 25	Oil and wipe clean carriage guide bar and plate.
6.	HI HF	Grease all metal to metal gear faces. Check for proper meshing or wear.
7.		Remove cover from head and clean solenoid wires with a small dry paint brush.

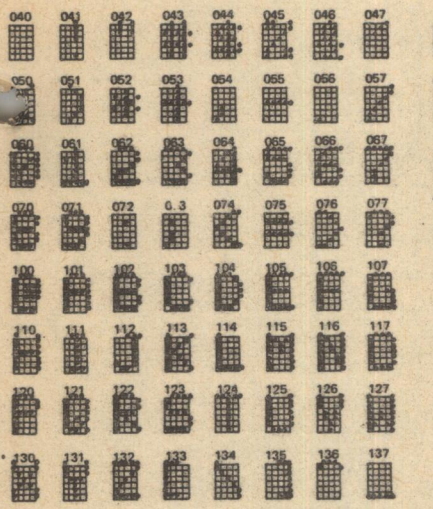
SPECIAL CONTROL CODES

Reception of any of the following control codes from the input device will cause a special printer action, as described below.

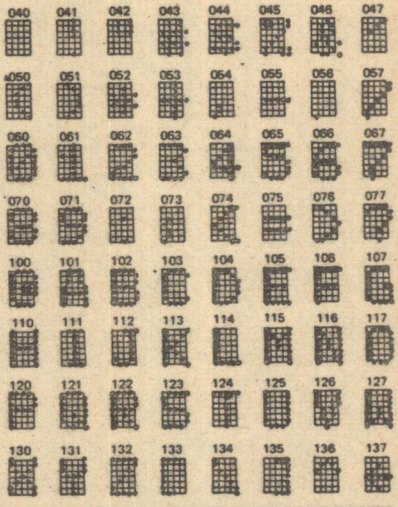
Function	Octal code	Description
BELL	007	Generates an audible tone, about two seconds in duration, in the speaker at the rear of the printer.
LINE FEED	012	Advances the paper one line.
VERTICAL TAB	013	Advances the paper until the next hole in Channel 5 of the VFU paper tape is reached.
FORM FEED	014	Advances the paper until the next hole in Channel 7 of the VFU paper tape is reached.
CARRIAGE RETURN	015	Causes the line of characters stored in the printer buffer to be printed. As a standard feature, an automatic line feed occurs after printing the line.
ELONGATED CHARACTER	016	Prints entire line of up to 66 characters as expanded characters (double width). NOTE: Because of the two print heads in the 102A, a line of elongated characters must be received in the following order: (1) first 33 printable characters, (2) 33 "don't care" characters, (3) next 33 printable characters, and (4) carriage return code.
SELECT	021	Selects the printer (i.e., makes it available to receive data).
DE-SELECT	023	De-selects the printer (i.e., prevents the printer from receiving data).
DELETE	177	Clears the buffer and initializes the printer electronics.

STANDARD CHARACTER SETS

STANDARD 5x7 CHARACTER MATRIX



STANDARD 9x7 CHARACTER MATRIX



USASCII CODE

$b_1 b_6 b_5$ Bits →					0_{0_0}	0_{0_1}	0_{1_0}	0_{1_1}	1_{0_0}	1_{0_1}	1_{1_0}	1_{1_1}
b_4 ↓	b_3 ↓	b_2 ↓	b_1 ↓	Column / Row	0	1	2	3	4	5	6	7
0	0	0	0	0	NUI	DLE	SP	0	@	P		p
0	0	0	1	1	SOH	DC1	!	1	A	Q	a	q
0	0	1	0	2	STX	DC2	"	2	B	R	b	r
0	0	1	1	3	ETX	DC3	#	3	C	S	c	s
0	1	0	0	4	EOT	DC4	$	4	D	T	d	t
0	1	0	1	5	ENQ	NAK	%	5	E	U	e	u
0	1	1	0	6	ACK	SYN	&	6	F	V	f	v
0	1	1	1	7	BEL	ETB	'	7	G	W	g	w
1	0	0	0	8	BS	CAN	(	8	H	X	h	x
1	0	0	1	9	HT	EM	)	9	I	Y	i	y
1	0	1	0	10	LF	SUB	*	:	j	Z	j	z
1	0	1	1	11	VT	ESC	+	;	K	[	k	{
1	1	0	0	12	FF	FS	,	<	L	\	l	|
1	1	0	1	13	CR	GS	-	=	M	]	m	}
1	1	1	0	14	SO	RS	.	>	N	^	n	~
1	1	1	1	15	SI	US	/	?	O	_	o	DEL

CONTROL CODES — STANDARD — OPTIONAL

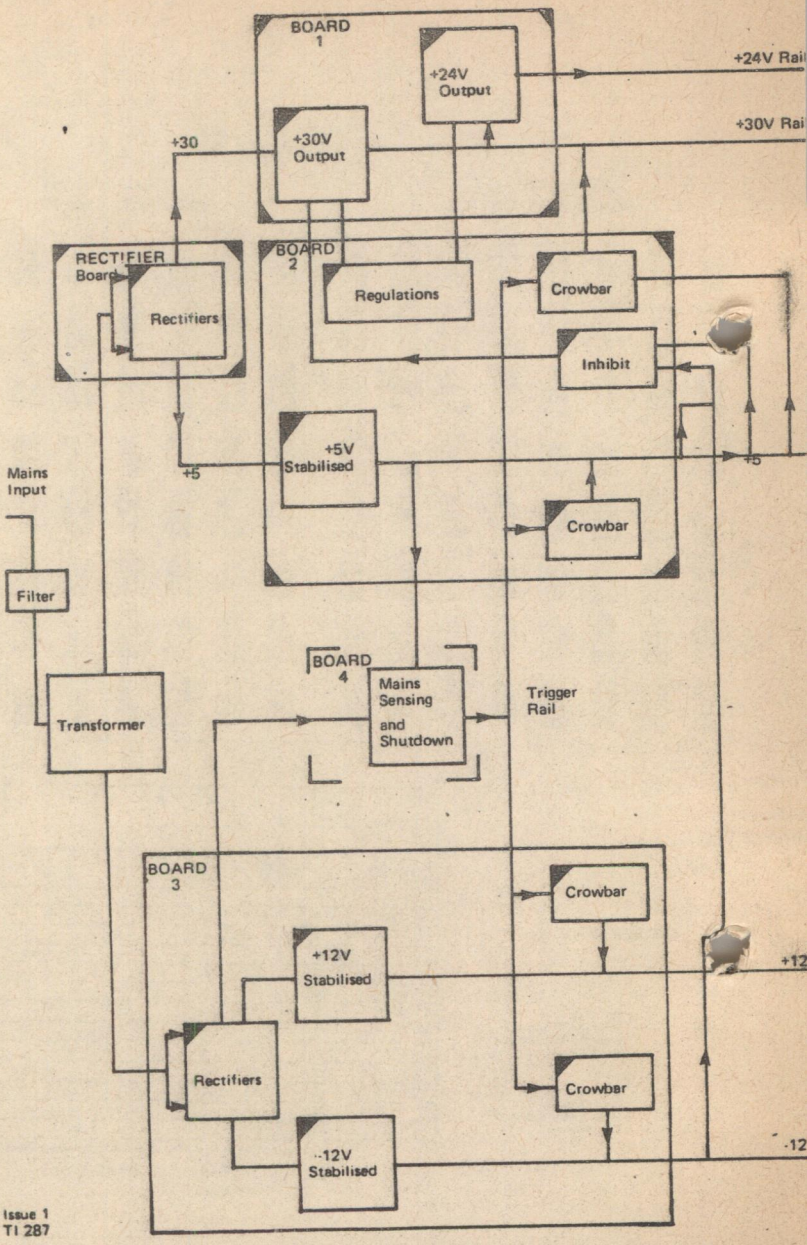
Notes:

1. ▭ Indicates control codes recognized by Centronics printers
2. Underscore (octal 127) is replaced by a back-arrow in the standard 9 x 7 matrix

No.

Text

P1



Stop

No.

Issue 1
TI 287

POWER SUPPLY BLOCK DIAGRAM **Fig. 1–11**

POWER SUPPLIES

POWER SUPPLIES

Introduction

The Nova power supply converts either 110V A/C at 60hz or 240V A/C at 50hz to a regulated, current limited 5V DC, -5V DC, +15V DC for the logic and memories, and an unregulated 6.3V AC for the real time clock (located on the scanner PCB).

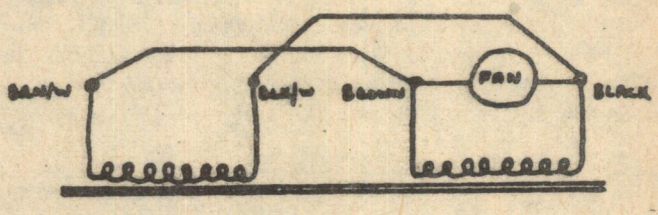
The PSU has a power monitor and restart option. The power supply interrupts the computer when it detects a line voltage failure (less than 80% of nominal) or stops the computer when the voltage sets too low for reliable operation. It issues a start pulse to the computer when the line voltage recovers.

The Nova 1200 has two power supplies. The top PSU provides +5V and -57 and feeds the logic for the upper PCB logic. The lower Power supply is identical and feeds +5 and -5 to the lower PCB logic and the +15V to the memories which is the only adjustable voltage. This voltage VMEM is critical for correct memory working. VMEM "tracks" with temperature thus ensuring a constant voltage over a wide temperature range.

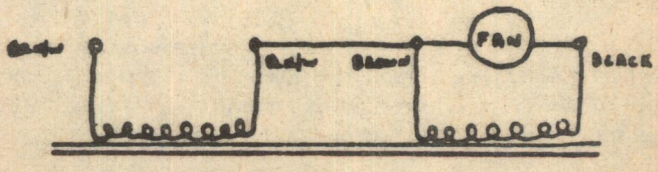
1.2 POWER SUPPLY CIRCUITS

110V AC or 220V AC are input through the power lead to a switch on the console S1 and then to transformer T1 in the PSU (Note: take care when re-fitting a power supply after removal as the Red and White cable often gets trapped between the PSU Chassis and CPU Chassis and causes shorts. Feed this cable from the underside of Nova chassis). The two primaries of T1 are wired in parallel for 110V AC and in series for 220V AC. Note that the cooling fan operates on 110V AC only.

Wire for 110V



Wire for 240V



The secondary of the transformer is wired to a full wave bridge rectifier which outputs approxim tely +30V DC (30-35VDC) into an RC filter, and subsequently to the +5V and +15V series pass switching regulators.

1.3 THE SERIES PASS SWITCHING REGULATORS

The series pass switching regulator acts like a multivibrator, which sets when it detects a low output voltage and resets when it detects a high output voltage. When the regulator is set it gates current from the 30V DC supply into an LC circuit and the load; when the regulator is reset the load draws all of its power from the LC circuit until the circuit is sufficiently exhausted to be recharged by the regulator. The frequency at which the regulator sets and resets varies from 0 to 25Khz depending upon the load.

There are two such regulators, one for the +15VDC and the other for the +5VDC and -5VDC circuit. Note that the outputs of these regulators are DC levels with about .51V ripple at frequencies which vary with the loads.

1.4 THE FUSES

The power supply has two 10 amp fuses, one between the power card and the switch S1 and the other just after the bridge rectifier. The first will blow if there is a short in the cabling to S1 the second will blow if the +15VDC or the +5VDC levels rise high enough to trigger an SCR) which then creates a short between the 30V supply and ground, this circuit works as follows:—

There are two Zener diodes one rated at 18V the other 6.2V. If the voltages rise to this they conduct firing an SCR. The total power supply current is then sunk through 3-1.5 ohm, 3 watt resistors and the SCR, this current surge then blows the 10 amp fast blow fuse S2. Experience has shown however that 9 times out of 10 if the SCR does fire the fuse does not blow quick enough, with the result that the Resistors and SCR cannot sustain the current through them and burn up generally taking with them the Zener diodes and Pass transistors SN 4399 and 4400. If the SCR has been found to have fired check all these components before switching on again.

Ensure that Resistors R14 and R15 are 47 ohm and 390 ohm respectively if not change to these values.

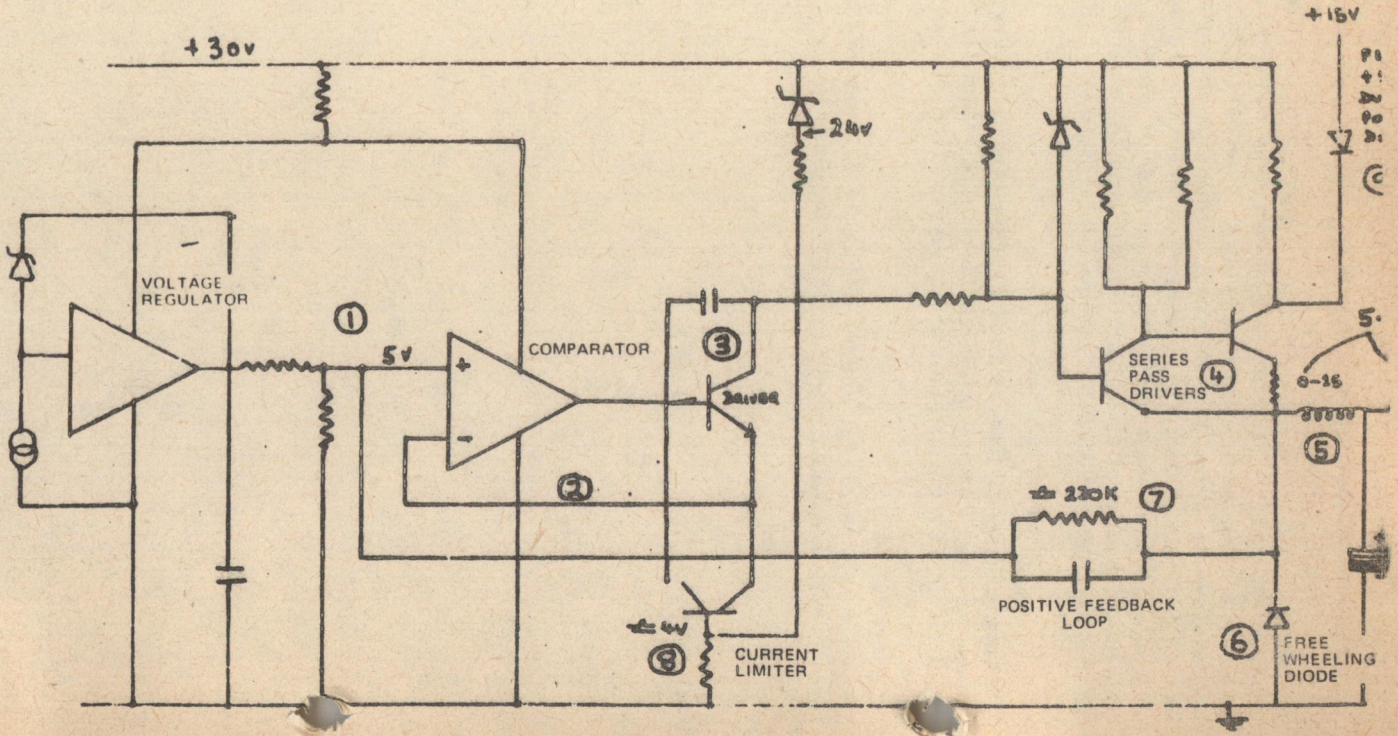
1.5 +5V SUPPLY

Fig. 1-1 shows a simplified schematic of the +5V series switching regulator. When the comparator senses a difference between the reference voltage (1) and the output voltage (2) it switches, turning on the driver transistor (3) and consequently the series pass transistor (4).

Current is shunted through the series pass transistor to the coil, output capacitor and load (5). The output voltage rises, reducing the error voltage to the comparator, which resets, turning off the driver (3) and consequently the series pass transistors. Now the load is supplied from the power stored in the L.C. Circuit. The back emf developed across the coil as a result of this switching is dropped across the free wheeling diode (6). Note that each time the comparator is forced to switch it is driven into saturation by the positive feedback loop which includes the 220K resistors (7).

The current limiter (8) turns on if the output voltage drops below about 4V, turning the driver (3) and subsequently the series pass transistors (4) off. The supply is latched in this state until power is removed and returned.

The diode at (9) feeds +15V into the +5V supply during power down, forcing the 15V to drop faster but the 5V to the IC's to hold on longer.


+30v
+15v
24v
VOLTAGE REGULATOR
1
5v
COMPARATOR
3
SERIES PASS DRIVERS
4
5
0-15
2
220K
7
POSITIVE FEEDBACK LOOP
6
FREE WHEELING DIODE
4v
8
CURRENT LIMITER

1.6 +15V SUPPLY

Fig. 1-2 shows a simplified schematic of the +15V series switching regulator, its operation is the same as the 5V circuit, but with the following differences.

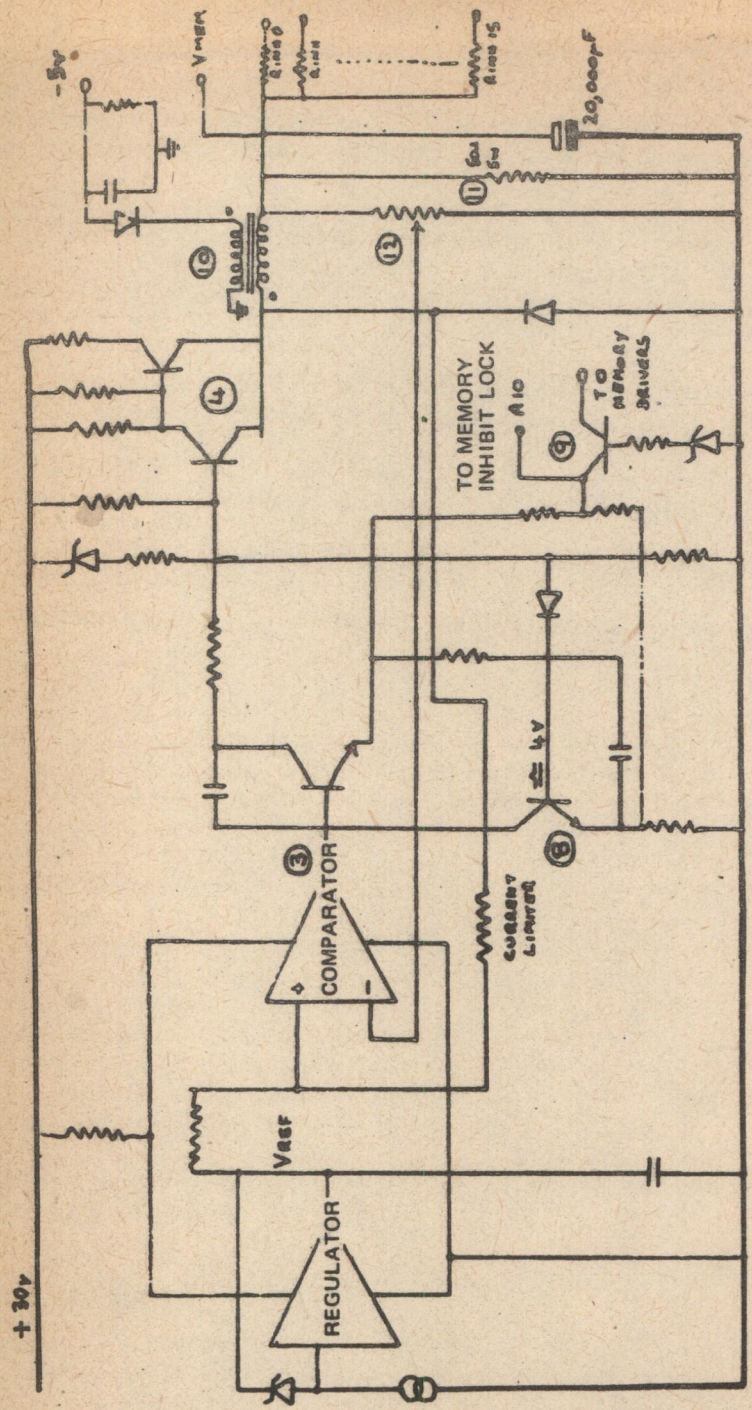
The current limiter (8) turns on if the output voltage VMEM drops too low, or if the current at either terminal at (9) (Memory inhibit and memory drive) is too high. When on, the current limiter turns off the driver (3) and subsequently the series pass transistors (4), latching the supply into this mode until power is removed and then returned.

The transistor at (9) will switch off when the +15V drops too low for the memory to function properly, thus removing power to the memory drivers.

The -5V is generated through the 3:1 transformer at (10). The 50 ohm resistor at (11) guarantees -5V (i.e. voltage across the coil) during no load.

The adjustable Resistor (12) is used for setting up VMEM.

The voltage temperature "Tracking" is performed by the voltage regulator.


-5v
VMEM
20,000pF
TO MEMORY INHIBIT LOCK
A10
TO MEMORY DRIVERS
4V
COMPARATOR
CURRENT LIMIT
VREF
REGULATOR
+30v

1.7 MEMORY POWER SUPPLY ADJUSTMENT VMEM

The memory power supply contains a control that changes the 15 volt output as the temperature changes. The voltage output against temperature is checked in the factory and should not normally require adjustment in the field.

To Check

Connect an electronic thermometer to the memory stack plate and fix down with tape (if more than one memory choose the lowest but one). Connect a digital voltmeter to Vmem (A10 on any memory slot). Run EXERCISER for at least half an hour.

Stop the CPU and monitor voltage and temperature. Check that it is within specification (Fig. 1).

To Adjust

Remove the 4 retaining screws on the lowest power supply. Turn off the Nova power and quickly pull out the PSU about 2 inches. A small pot is then visible. Turn a FRACTION (clockwise increases Vmem), push back PSU and switch on. Re-monitor voltages and temperature.

Once adjusted EXERCISER should be run for at least an hour before assuming the memory is OK.

Note: Ensure that all PCB's are in position and that the monitoring takes place with the chassis back in the cabinet.

Relationship between VMEM AND TEMPERATURE

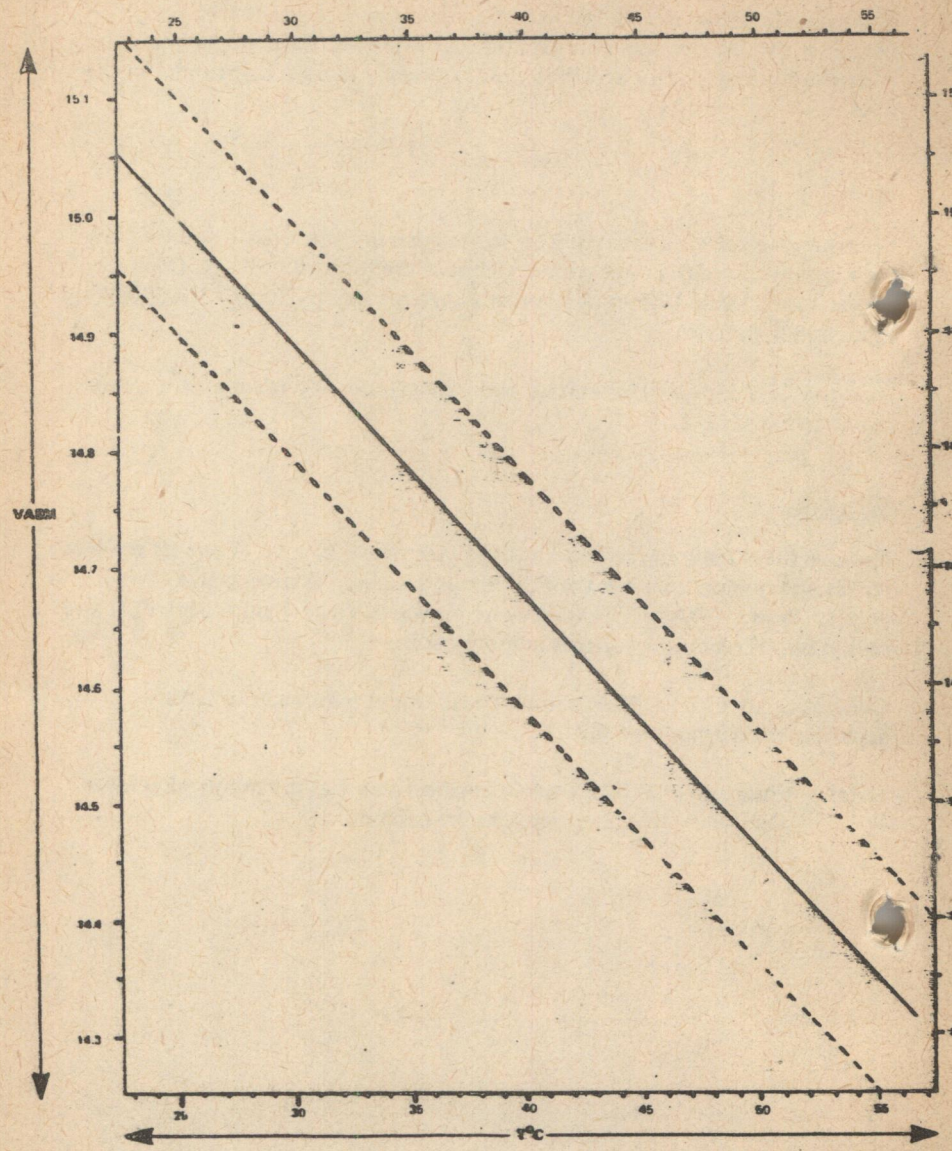


TABLE 1–1

OUTPUT VOLTAGES OF THE NOVA PSU

Output Voltage Level Name	Output Voltage	Max I	Usedon	Remarks
+V LAMP	14.5→15.1 VDC	8A	Console Lamps	Full wave rectified & over voltage protect Regulated
+ VMEM	14.5→15.1 VDC	8A	XY Drivers	"
+5V	5.2V→5.4DC	10A	IC Logic	"
-5V	-5V→ -7VDC (.15V Ripple)	1A	Sense Amplifiers	Over current protected by DIODE
RINH ⟨0,15⟩	14.5→15.1 VDC (.15V Ripple)	760ma each	Inhibit Drivers	Full wave over voltage protected Regulated. Resistors mounted on main frame at rear of supply.
50 KHZ	6.3 VAC	500ma DC	Real Time Clock	Same frequency as input voltage
B84	14.5-15.1 VDC	3A	Memory Drivers	Turns off memory drivers when +15V drops to 12VDC
VINH (A10)	14.5-15.1 VDC	3A	Memory Inhibit Logic	Current Limited

2.1 POWERFAIL

Three signals are sent to the CPU card from the two Nova Power supplies.

1. +5 OK (CPU A8. PSU 50) from lower PSU.
2. MEM OK (CPU A9. PSU 50) from top PSU.
3. $\overline{\text{PWR FAIL}}$ (CPU A5. PSU 23) from top and bottom PSU's.

If interrupts are enabled the power fail line causes the CPU to interrupt to location zero as for a normal interrupt. The power fail can be sensed by an I/O skip on D one with CPU code 77. The accumulators, carry and location zero should be saved and location zero replaced by a jump to a power fail restart routine. The program should then Halt waiting for power to be lost.

If interrupts are not enabled or the power fail interrupt has taken place the MEM OK line will reset. This resets RUN.

The time between the PWR FAIL line going and MEM OK going is at least 3 ms.

2.2 POWER ON RESTART

The CPU key must be in the LOCK position for automatic restart to function.

When the +5 OK comes up it generates a CPU reset pulse.

When Mem OK and $\overline{\text{PWR FAIL}}$ have reached a '1' (Fig. 2–1) after power restoration, monostable U1 fires for 20us. The output of this clocks U2. The D input of U2 (Restart enable) comes from the key switch on the control panel. The output of U2 is RESTART. $\overline{\text{RESTART}}$ goes to U3-5 to generate KEY SEEN. This sets the CPU into the KEY major state. KEY sets RUN. KEY. RESTART Cause IR0, 5, 6, 7 to be reset. After the KEY cycle the MBO is clear, FETCH is set and a memory cycle starts from location 0 (which was set to a jump to the power fail restart routine during power fail).

Fig. 2–1 DATA GENERAL CPU Additional Logic

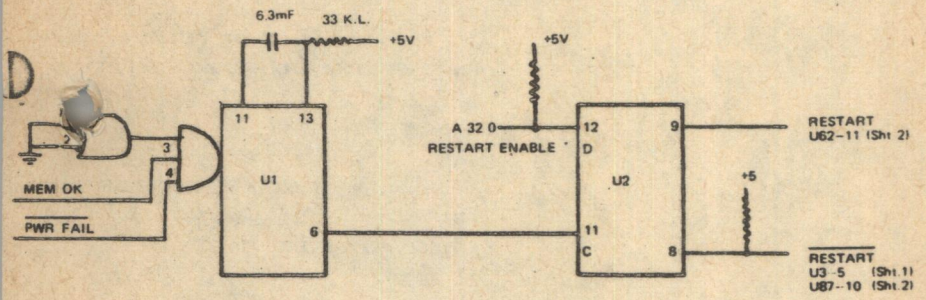


TABLE 2–1

OUTPUT SIGNALS OF NOVA PSU POWER FAIL MODULE

Signal Name	Signal Function
$\overline{\text{PWR}}$ $\overline{\text{FAIL}}$	Sets POWER LOW in the processor when the line voltage drops to 80% of nominal voltage.
MEM OK	Resets RUN and stops the computer when the +V mem voltage goes too low for the memory to function reliably.
+5 OK	Causes a RESET pulse in the computer when the +5VDC has risen to 4.4VDC

3.1 INTRODUCTION

There are two types of dynage supply in use. When installed in the rack they are essentially the same.

The output is +15V and -15V which is used purely to supply the disc drive. An adjustment is provided should the supply require it. On the later model there is a second pot for balance but when installed in the rack this faces the side of the cabinet. The balance should not require adjustment in the field.

4.1 TERMINAL POWER SUPPLY

The terminal power supplies provide a stabilised +5, +12 and -15V DC to the terminal.

The power supply is mounted in the rear of the terminal. Three power supplies are in use:

1. Tresco

   This can be identified by the fact that it has two mains transformers.

2. Elasco

   This has only one transformer and the layout is neater.

3. Redifon

   This is fitted to the later terminals built by Redifon but is electrically the same as the Elasco.

MK. 2 KEYSTATION POWER SUPPLY (WEIR)

CIRCUIT DESCRIPTION

As all three circuits are of similar configuration, only the +5V circuit will be dealt with in detail and is to be read in conjunction with circuit diagram given on page 3–69 of System Logic Manual RDS–261–10.

The mains supply is fed into the toroidal transformer T1, transformed to an appropriate level by a centre-tapped secondary winding, fed onto the printed circuit board via pins 3, 4 and 5, through the secondary protection fuses FS2 FS3 then full wave rectified by D3 and D4 into a smoothing capacitor C1. This unregulated d.c. is then fed to the collector of the series pass element TR4. A suitably transformed boost winding feeds an alternating voltage via pins 1 and 2 onto the printed circuit board, through a protection fuse FS1 and full wave rectified by the bridge formed by diodes D1, D2, D5 and D6. This boost d.c. level is then cascaded with that across C1, fed to another smoothing capacitor C2 which then feeds the control and crowbar circuits.

A voltage regulator, IC1, maintains the required output level which is set by the potentiometer chain formed by RV1, R1 and R2 and sensing takes place at the output connector pins J1/2 and J1/4.

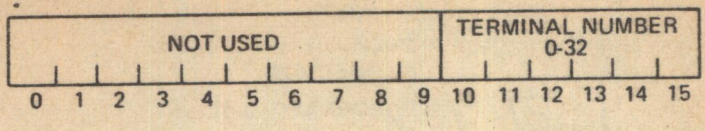
Overcurrent protection is achieved by comparing the voltage developed across the sense resistor R9 with that across R5.

At the required load current level, R6 is selected to start turning on the current limit transistor in IC1 and the output exhibits a re-entrant characteristic i.e. the load current reduces as the output voltage falls. When the output is short circuited the load current is at such a level to keep the power dissipated in TR4 to a safe level and to prevent 'latch up' occurring i.e. allows the output to function normally when the overload is removed. Overvoltage protection is provided by a crowbar circuit. As the output voltage rises the V_{be} of TR5 increases until such time that TR5 starts turning on. The voltage across R12 rises and when sufficiently high fires SCR1 and the output collapses. R38 limits the gate current of SCR1 to a safe level and with C5 provides a short time delay to prevent the circuit tripping unnecessarily.

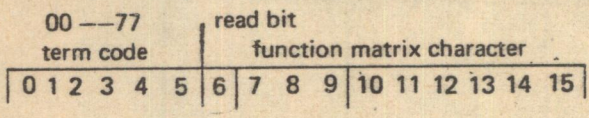
SCANNER/TERMINAL

TERMINAL & PER TERMINAL
TERMINAL MULTIPLEXER ACCUMULATOR CONTENTS

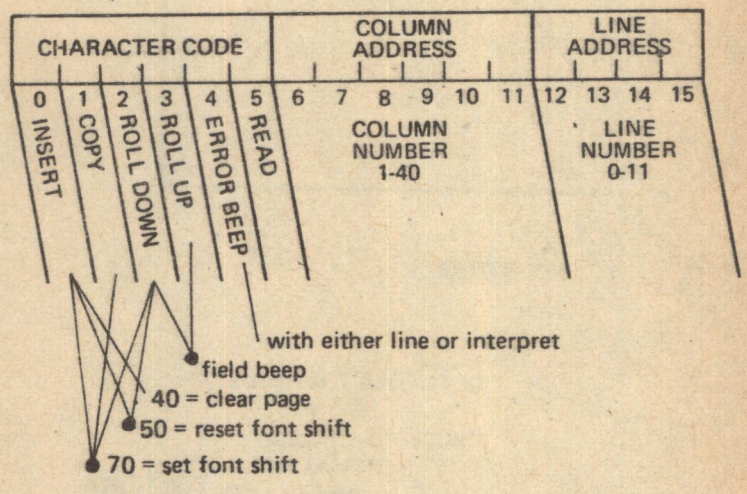
DOA, AC, 60



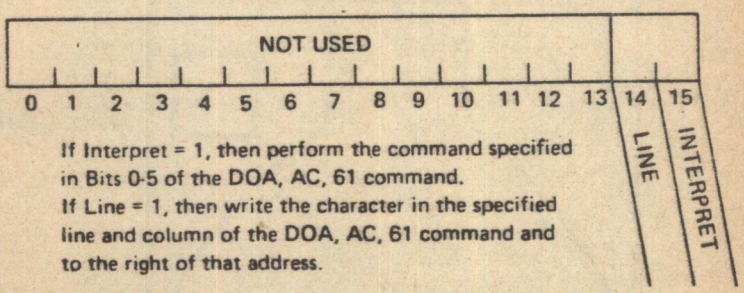
KEYSTROKE AS SEEN IN LOCATION 400/kystr bfr.



DOA, AC, 61



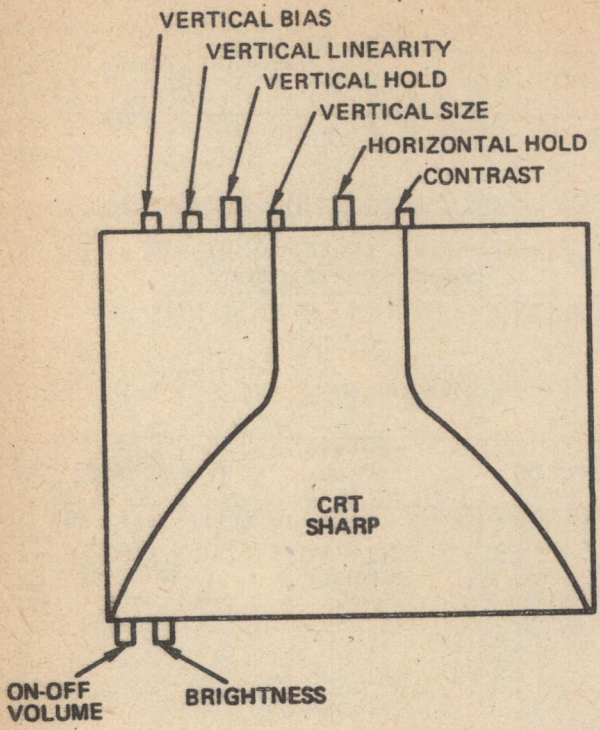
DOC, AC, 61



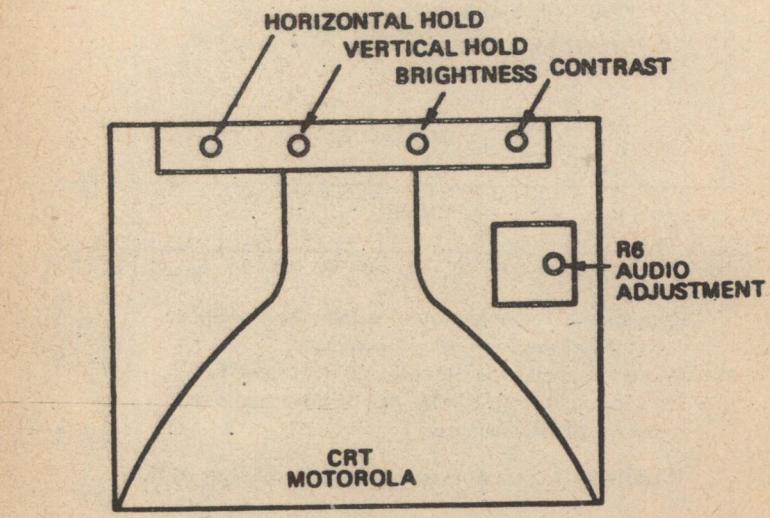
If Interpret = 1, then perform the command specified in Bits 0-5 of the DOA, AC, 61 command.
If Line = 1, then write the character in the specified line and column of the DOA, AC, 61 command and to the right of that address.

If both are 1's, command = clear page or font shift.

SHARP T.V. ADJUSTMENTS



MOTOROLA T.V. ADJUSTMENTS



KEYPUNCH KEYBOARD CODES

The following codes are used for the lower case characters:

Code	Character
00	X
01	Z
02	S
03	A
04	W
05	Q
06	@
07	%
10	V
11	C
12	F
13	D
14	R
15	E
16	*
17	<
20	space
21	B
22	H
23	G
24	Y
25	T
26	spare
27	—
30	N
31	M
32	K
33	J
34	I
35	U
36	/
37	spare
40	,
41	.
42	L
43	O
44	P
61	AUTO
62	RESET
63	INS
64	DEL
65	DUP
67	HELP
71	COR
73	FIELD RELEASE
74	→
75	←
76	LOC RET
77	REL

The following codes are used for the upper case characters:

Code	Character
00	?
02	>
04	—
05	+
06	#
07	'
10	=
11	"
12	;
13	:
14	¢
15	)
16	$
17	.
21	!
22	,
23	¬
24	|
25	≠
26	spare
27	—
30	(
31	7
32	5
33	4
34	2
35	1
36	0
37	spare
40	8
41	9
42	6
43	3
44	&

Used with upper case keys:

Code	Key
1	NUM
2	ALPHA
4	PGM
5	RCD
6	FLD

TYPEWRITER KEYBOARD CODES

The following codes are used for the lower case characters:

Code	Character
00	0
01	1
02	2
03	3
04	4
05	5
06	6
07	7
10	8
11	9
12	—
13	.
14	P
15	;
16	/
17	I
20	space
21	Q
22	W
23	E
24	R
25	T
26	Y
27	U
30	L
31	A
32	S
33	D
34	F
35	G
36	H
37	J
40	,
41	Z
42	X
43	C
44	V
45	B
46	N
47	M
50	O
51	K
61	AUTO
62	RESET
63	INS
64	DEL
65	DUP
67	HELP

Code	Character
71	COR
73	FIELD RELEASE
74	→
75	←
76	LOC RET
77	REL

The following codes are used for upper case typewriter characters:

Code	Character
00	)
01	+
02	@
03	#
04	$
05	%
06	¢
07	&
10	*
11	(
12	—
13	.
15	:
16	?
20	
21	
22	
23	
24	
25	≠
26	
27	|
32	>
33	<
35	¬
36	'
40	;
43	"
44	=
45	!

Used with upper case keys:

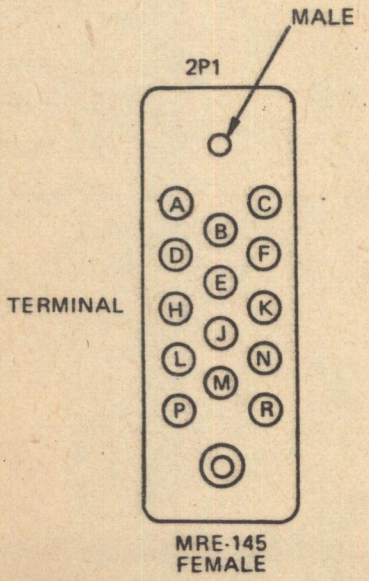
Code	Key
1	SHIFT
4	PGM
5	RCD
6	FLD

TERMINAL POWER SUPPLY OUTPUT VOLTAGES

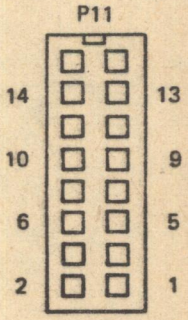
Pin A +5 V	Red
Pin C +12 V	White
Pin D GND	Green
Pin E -15 V	Purple

CABLE CONFIGURATION TERMINAL TO PERTERMINAL CAGE

Signal Name	Terminal 2 PI Pin No.	Perterm Board P11 Pin No.	Wire Color
Data In	A	11	Red
Data In	C	12	Black
GRD	B	3	Brown
GRD	F	4	Black
GRD	J	5	Black
Xmit Req	P	6	Yellow
GRD	D	9	Black
MBZ	L	8	Green
GRD	D	9	Black
Xmit Enable	H	10	Blue
Data Out	N	1	White
Data Out	R	2	Black



MRE-145
FEMALE



PER TERM BD.

AMP 86262-4
FEMALE

CRT code for displayable characters:

00	Space	30	Q	60	Ø
01	A	31	R	61	1
02	B	32	!	62	2
03	C	33	$	63	3
04	D	34	*	64	4
05	E	35	)	65	5
06	F	36	;	66	6
07	G	37	¬	67	7
10	H	40	–	70	8
11	I	41	/	71	9
12	¢	42	S	72	:
13	.	43	T	73	#
14	<	44	U	74	@
15	(	45	V	75	'
16	+	46	W	76	=
17	|	47	X	77	"
20	&	50	Y	CRT code for	
21	J	51	Z	Contr. Chars.	
22	K	52	≠	15	CR
23	L	53	,	01	Fld Rel
24	M	54	%	00	Rel
25	N	55	–	75	→
26	O	56	>	74	←
27	P	57	?		

ENTREX DATA SCOPE EXERCISOR

PRELIMINARY RELEASE

OPERATION PROCEDURE

Originator: F. Krupecki **Date: 3/21/75**

For cabling and code set info, refer to Chap. 7, F.E. Ref. Manual, 02083.

Switch Functions

A. Input/Output refers to exercisor, i.e. input is to exercisor, output from exercisor.

B. Single/Continuous continuously outputs contents of char, column, and line switches to data scope in cont. mode.

In single mode it halts after the single output.

In cont. mode, you will see cursor flashing on next column of selected line; it will not appear in single.

C. Auto/Manual sequentially fills the screen with a full complement of EBCDIC characters when in the auto mode.

In manual mode you must manually select character, column, and line.

D. Character —— Enter octal code from FE Ref., pg. 7—6 temp for characters output to data scope in a manual operation.

These switches are used to encode the function to be output to the data scope in "Interpret" mode, also, according to the diagram at the center of F.E. Ref., pg. 7—1..

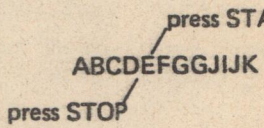
E. Line = octal value of selected line for a manual operation.

F. Column = octal value of selected column for manual mode.

G. "L" This function is used only when Interpret function is not selected. In output, continuous, and manual mode will fill the selected line with character switch selection when "L" is raised.

H. "I" When the I switch is raised, performs the function interpreted in bit positions corresponding to bits 0 —— 5 of the center drawing on page 7–1 of the FE Ref. Manual.

NOTE: If in auto mode and cycling through the EBCDIC character set, you depress "HALT", and then depress "START", the first character will not increment as in the below example:



NOTE: When in auto and single modes, you will cycle through EBCDIC characters only after pressing START, as follows:

original display:	XXXXXXXXXXX
depress START:	XOXXXXXXXXX
release START:	XOXOXXXXXXX

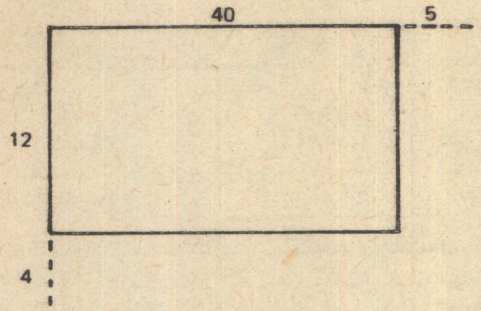
NOTE: For additional information on KEYBOARD to EXERCISOR operation, refer to ENTREX Data Scope Exercisor Theory of Operation (p/n 02271) ER # 578, page 5; and Test Procedure for Data Scope Exercisor (p/n 02272) ER #578A and FE Ref., page 7–3.

NOTE: The exercisor is effective in running a REMOTE RTA site (need twisted pair connector). It is suggested that short cables be made up with proper connectors for ease of testing.

MK1 TERMINAL DESCRIPTION

The terminal consists of a TV, power supply (+5, 0, -15V), keyboard and logic assembly.

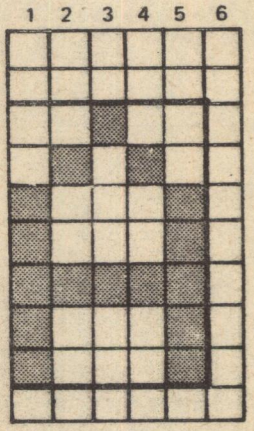
The character set is 64, displayed on a screen 40 characters wide by 12 deep (480).



5 characters extra to allow for retrace to left (slow retrace).

4 characters extra to allow for retrace to top. (fast retrace).

Each character occupies a 5 x 7 matrix within a 6 x 10 matrix

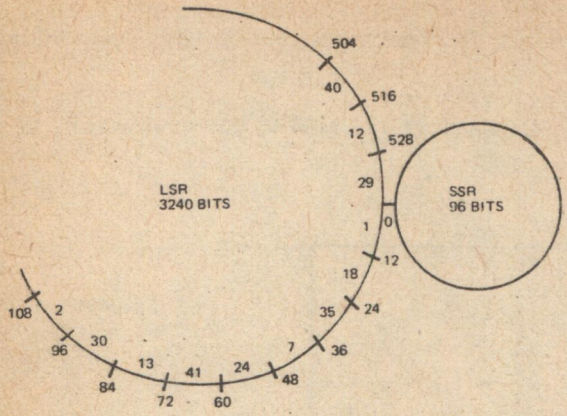


The spare places are for character separation. The yoke on the TV is turned through 90° and the coil wires poled over so the trace runs down the screen.

Each trace down the screen needs 12 + 4 = 16 characters. Each character has a 6 bit code so we need 16 x 6 = 96 bits of information for each trace. Each 6 bit character is decoded to give 10 bits in the required pattern. Each character must be repeated 6 times to give the 6 x 10 matrix. To hold the information for each trace we have a 96 bit short shift register (SSR).

To hold information for the whole screen we need 12 x 45 x 6 bits = 3240, this is held in the long shift register LSR.

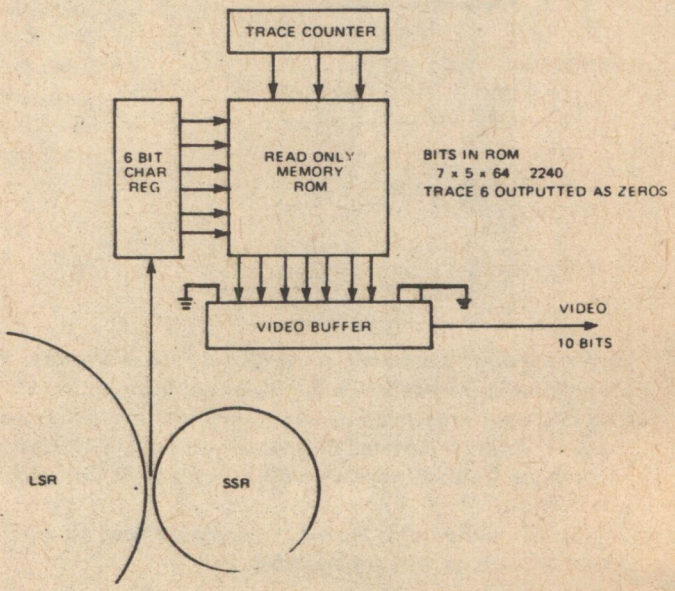
Relationships between LSR and SSR



Starting at column 1, character zero, 16 characters are loaded into SSR (last four are in fact the first four from column 18 but these are blanked off on the screen during retrace). By the time the first column of characters has been displayed the trace has gone down 6 times and the SSR has also gone round 6 times. This is 6 x 16 = 96 characters. The LSR has also stepped on 96 characters and is lined up ready to give column 2 to the SSR.

From this it can be seen that the columns are not in order on the LSR. The column sequence on the LSR is n + 1 = n + 17 (-45 if $\geqslant$ 45).

LSR and SSR to Video



As the first character is read into the SSR it also goes into a 6 bit character register. This in conjunction with the trace counter addresses a RCM to give a 7 bit output for the character to the screen. The video buffer is 10 bits 1, 2 and 10 are always zero.

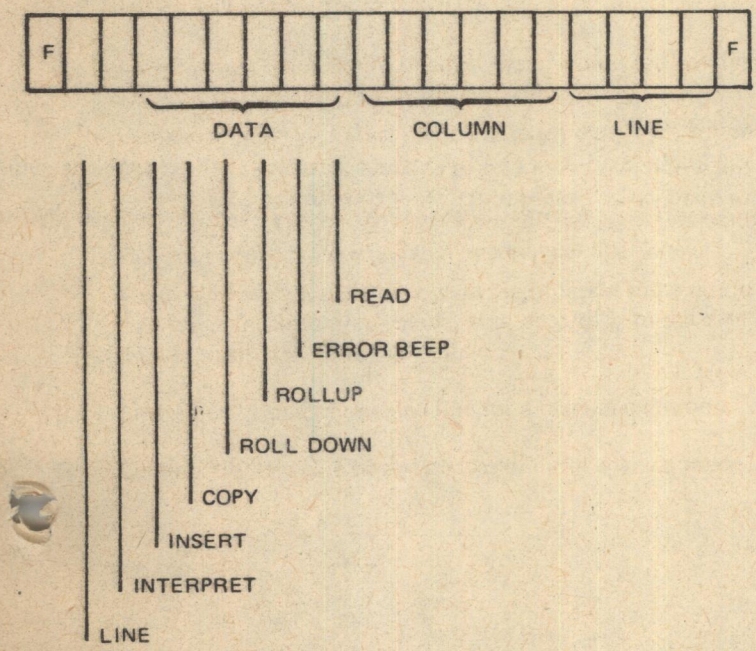
The trace counter counts 0–5. It is incremented by the screen cycling line counter (SCLC) counting to 16. When the SCLC reaches 12 the screen is blanked to allow for the fast retrace.

Column Control

As the SCLC is counting a cycling character counter (CCC) is counting. This counts in 17's but resets to zero if the count gets greater than 45. This keeps track of the column number across the screen. When the count reaches 40 the screen is blanked off to allow for the slow retrace.

Output from Scanner to Screen

A 20 bit serial word is received from the scanner



The 6 data bits are either decoded as data or as control functions depending on the state of the interpret bit.

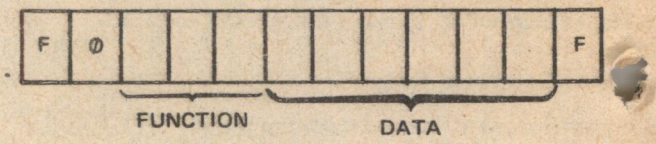
After shifting the 20 bits in the two framing bits (F) are checked tn see that they are set as a check on a correct data load.

As soon as the word is shifted in, the column and line data is compared with the appropriate counters. When the two agree the LSR must be set up to receive the data and it is clocked into the LSR in place of the original data.

Keyboard Input

The keyboard is a scanning encoder. A 6 bit counter drives a 1 of 8 decoder and an 8 input Multiplexer. A switch closure connects one of the decoder outputs with one of the multiplexer inputs and when the count is correct, a key closure is indicated by Eureka.

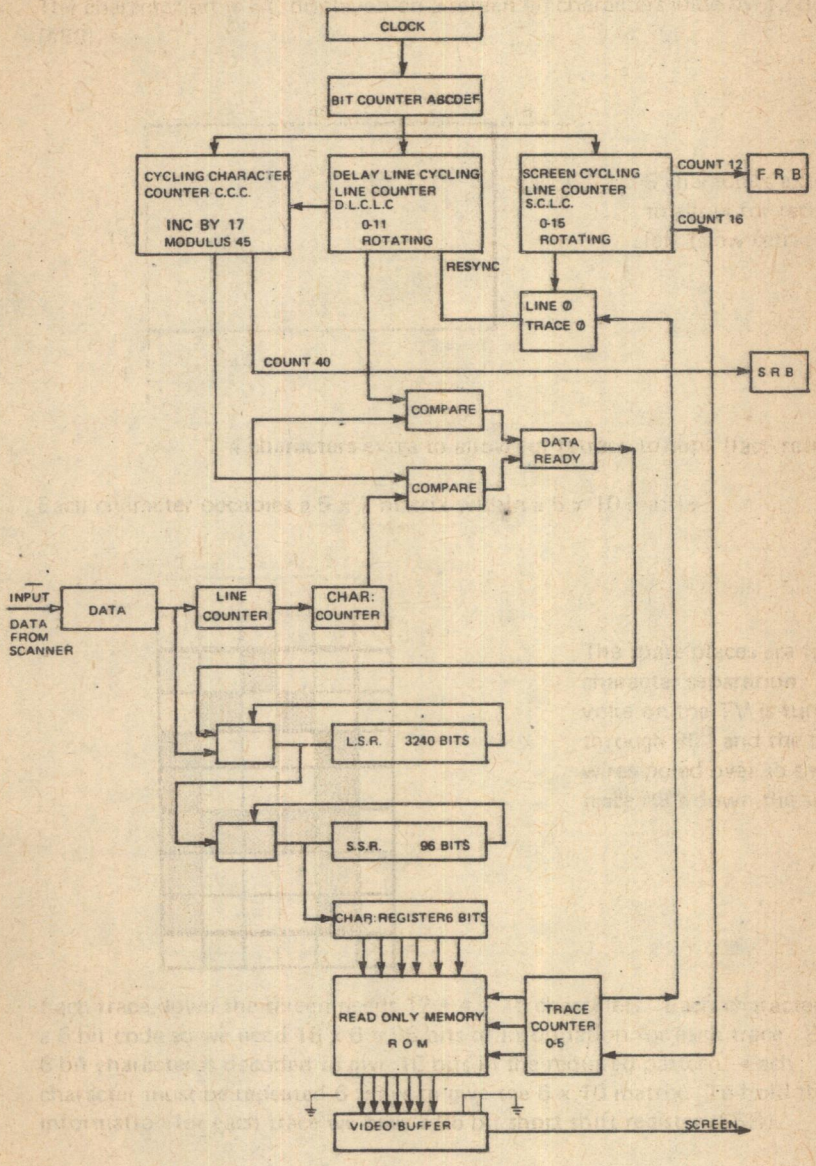
A one shot is fired to take care of switch bounce and a transmit request is sent to the scanner. When transmit enable is received a 12 bit serial word is sent to the scanner. This includes 2 frame bits.



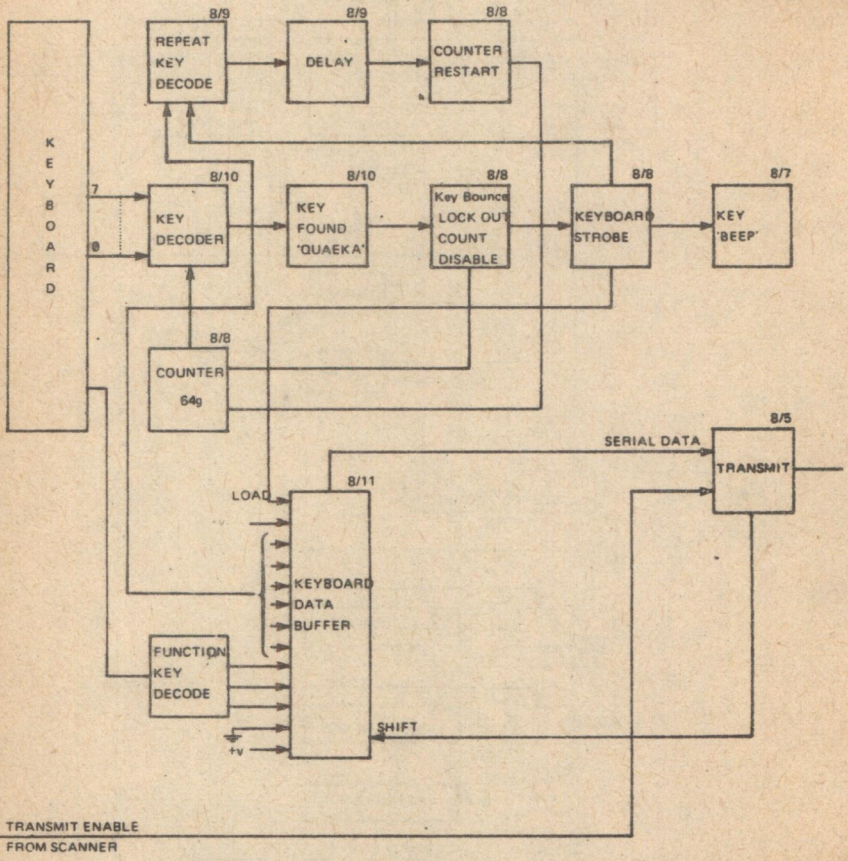
Terminal Busy

If the terminal is asked to output a character, it goes busy until the counters have matched and the character loaded onto the LSR.

MK1 TERMINAL BLOCK DIAGRAM OUTPUT



MK1 TERMINAL BLOCK DIAGRAM INPUT



TERMINAL MK2

The Terminal MK 2 is a horizontal scan keystation which is software compatible with the Terminal MK 1 and presents the same display of 12 lines of 40 characters each. Apart from the fact that the terminal VDU deflection coils are turned through 90 degrees to enable a sweep in the horizontal direction. The only other major difference between MK 1 and MK 2 is that it has two character generators and can display 128 different characters. The construction of the terminal is similar to MK 1, incorporating all logic circuits on one pcb.

The terminal logic consists of two main sections:

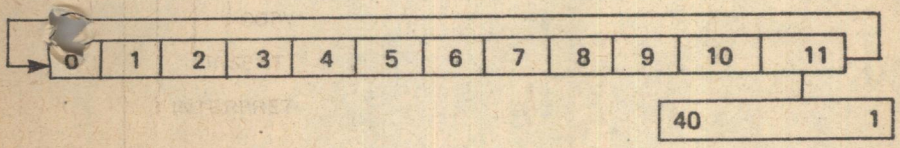
1. Scanner and Per-terminal cards
2. Display Terminal

Section 1 of the logic performs the same function as the MK 1 terminal. It is the I/O device which transmits and receives the serial data from up to 32 keystations. However, the display section receives the serial data from the scanner, converts it from serial Manchester code to binary code and formats it for refreshing memory and display on the CRT.

The Display Memory is divided into two sections:

1. Page Memory with capacity of 480 seven bit characters.
2. Line Memory with capacity of 40 eight bit words.

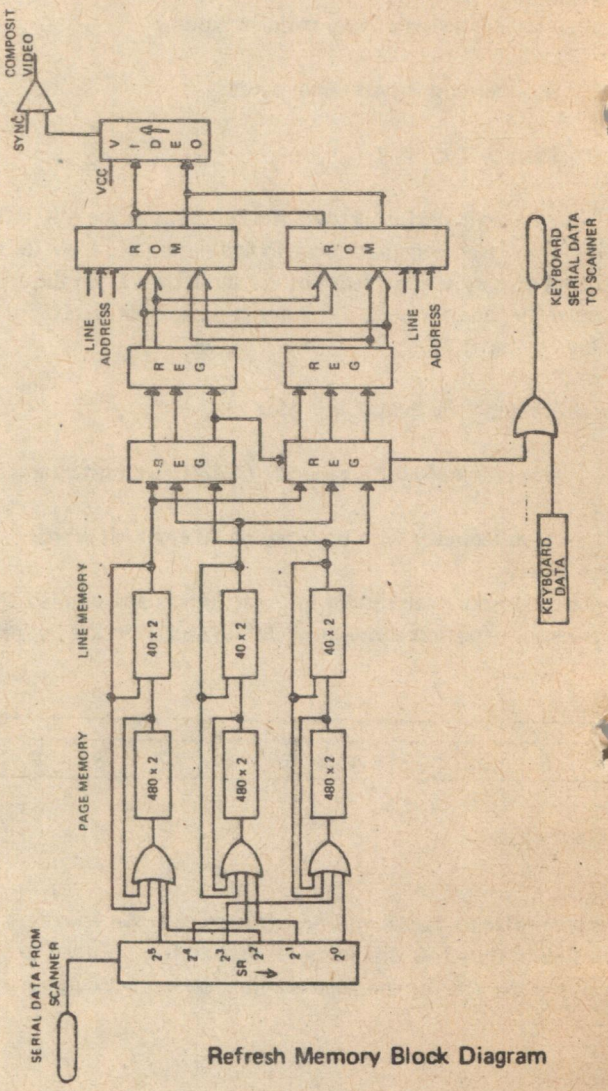
Both types of memory are similar in construction and employ shift register logic. The following illustration shows how data is stored in the page memory.



The numbers refer to displayed lines. During each sweep across the display unit, one line of data (40 characters) is shifted from output to the input. Therefore it takes twelve sweeps for the page memory to be recirculated one time.

Assuming, at a certain time line 5 is at the output section of memory, after sweeps, line 6 will replace line 5 in the output section. Thus it follows that data at the output section of the memory will process one line of characters every 11 TV sweeps, 7 sweeps for the 7 character dots and 4 sweeps for the space dots between the lines of characters. As each line of characters is disp the next line of characters is in position to be transferred from the page me to the line memory.

Each character is composed of a 5 x 7 dot matrix in 6 x 11 field. The chara are displayed by tracing out lines of dots across the face of the TV screen.

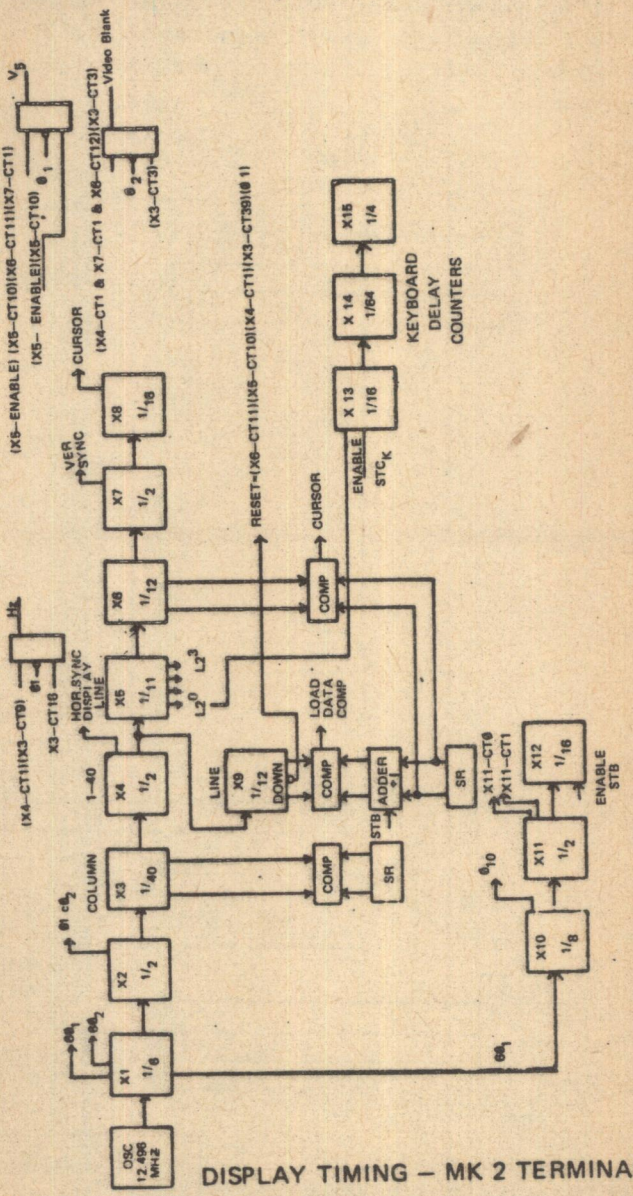


Refresh Memory Block Diagram

Issu

Display Timing

The following illustration shows a block diagram of the display timing. X numbers refer to binary counters. All counters either start at zero and count up to a binary number one less than it is to divide by or start at a number above zero and count up to 15. In the later case, if the counter is to be divided by 11, the counter will count from binary 5 to 15 and then is forced back to binary 5 via the load capability of the chip.

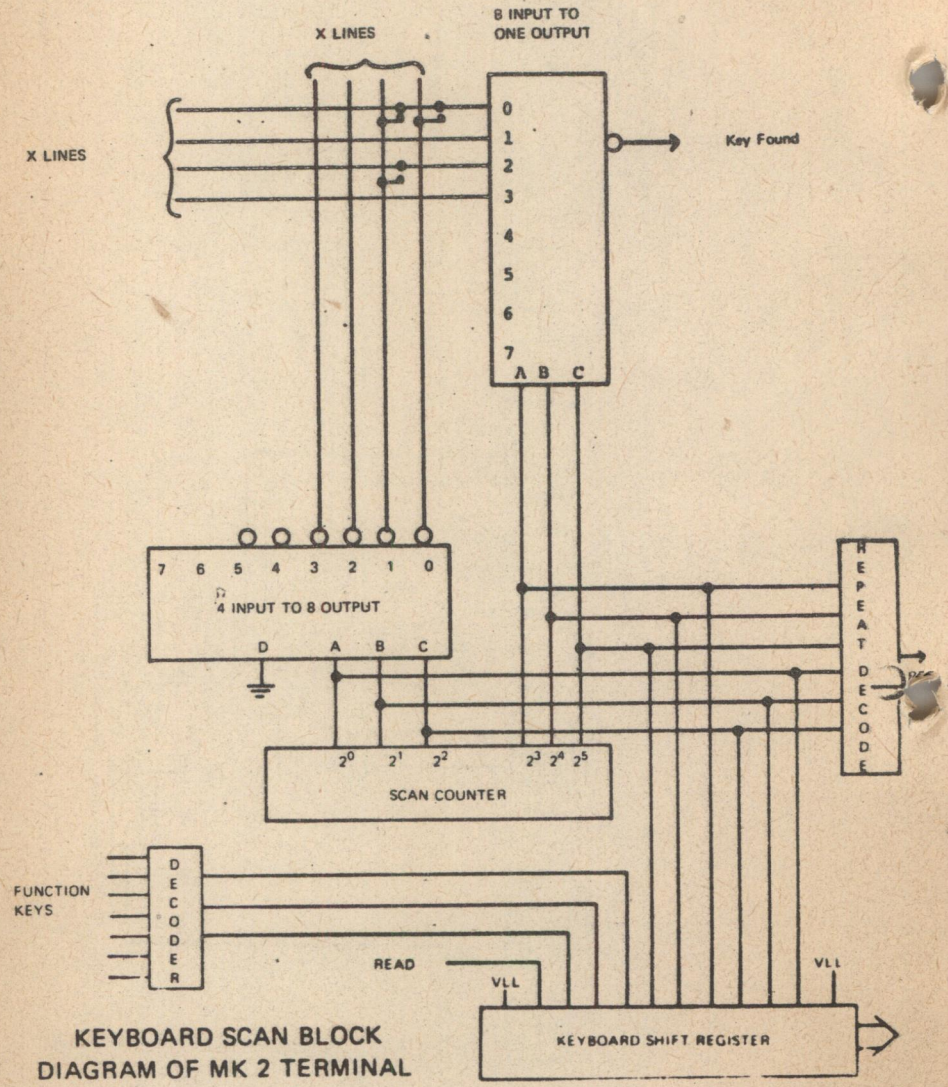


DISPLAY TIMING – MK 2 TERMINAL

Keyboard Input Scan

The following illustration shows a block diagram of the Keyboard Scan logic. The scan techniques are similar to MK1 terminal. Up to 64 keys can be used with the scanner. When a key is pressed, a connection is made between an x line and y line. The eight lines are connected to the BCD to decimal decoder and eight lines are connected to the eight inputs of the multiplexer.

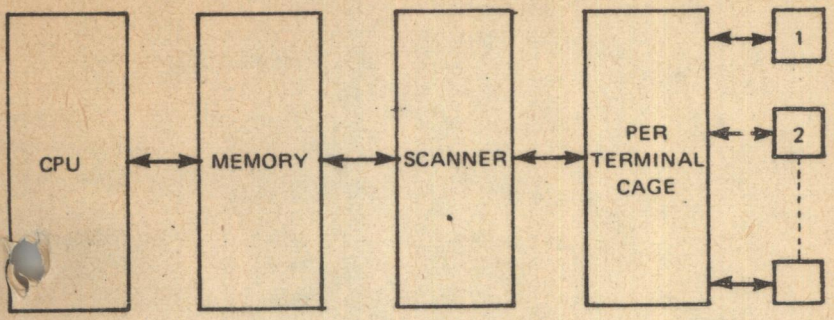
As the scan advances, it gates one of the y lines to the output of the multiplexer. The three MSB of the scan counter determines which of the inputs is to be gated to the output. The three LSB of the scan then select each of the x lines in succession.



KEYBOARD SCAN BLOCK DIAGRAM OF MK 2 TERMINAL

SCANNER

The scanner receives data from the CPU, transmits it to a terminal (Output), and receives data from a terminal and transmits it to memory (Input).



Search and Input:

The states of two flip flops determine the mode of the scanner:–

Search	Input	Mode
1	Ø	Searching terminals for a request.
Ø	1	Input keystroke from terminal to scanner and send to memory.
Ø	Ø	Output a character to a terminal.
1	1	Illegal. This can only occur under power up or fault conditions.

Device Codes:

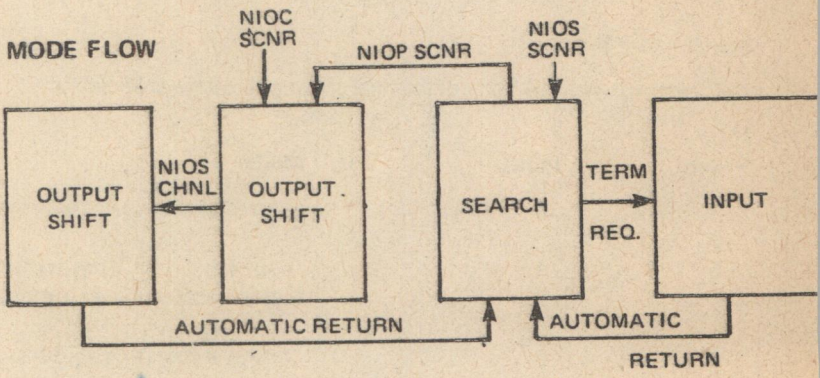
The scanner board has three device codes:–

60 SCNR.
61 CHNL.
64 Real Time Clock.

Mode Control using these device codes:

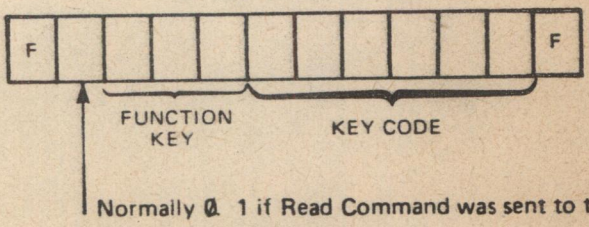
	60	61	64
S	Set Search Clear Input	Start Output Shifter.	Set RUN.
C	Clear Search. Clear Input	Clear ICA overflow and Interrupt Req.	Clear Done Clear Interrupt Req.
P	Set Scanner Stop Request	Clear Input Error	Clear Done Clear Interrupt Clear Run
BUSY LINE	SEARCH + INPUT + OUTPUT SHIFT	Selected Terminal Busy	RUN set
DONE	$\overline{\text{OUTPUT SHIFT}}$	ICA overflow	Timer Done

MODE FLOW



Search/Input Mode:

The scanner acts like a big 64 way rotating switch which goes round looking at each terminal for 2.4uS. If, whilst this "window" is open, a request is seen from the terminal the scanner is put into input mode and 12 bits from the terminal are shifted serially into the buffer.



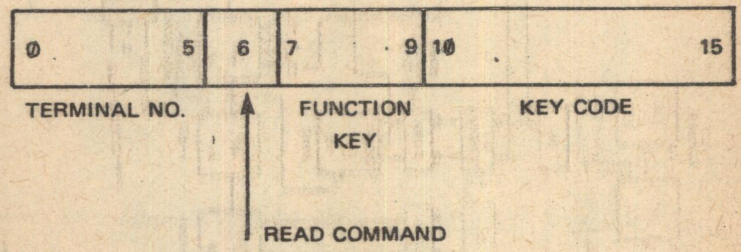
When both frame bits (F) are set the word is considered loaded. If, after 115μS the frame bits are not set, "frame in error" is produced, and the scanner goes back into Search mode. A normal transfer takes 38μS.

As soon as the word is loaded a Data Channel Request (DCHR) is generated and, when the acknowledge (DCHA) is received from the CPU, the input core address (ICA) is put on the data lines to the memory.

The ICA is the address in memory into which the keyed data is loaded. This is dedicated as 400_8 to 777_8. After each data transfer the ICA is incremented by one. The ICA can be reset to '400 by DOB CHNL. The ICA can be examined with DIB CHNL. ICA overflow is set every 64 characters (77_8) and an interrupt is generated.

In the Seecheck system the interrupt facility is not used and once started the software compares the memory address of last keystroke with the current value of ICA (DIB CHNL). If there is a difference then the software takes the keystroke data out of the buffer.

After the memory address has been sent the CPU replies with DCHI, and the 16 bit data word is sent to memory. The data word is the same as that shifted from the terminal with the addition of the number from the scanner counter.



After completing the transfer the scanner is restarted in Search mode.

Output Mode:

Before output can take place the scanner has to be switched from Search to Output Idle. This is done with NIOP SCNR. The scanner then has to be checked to see that it has in fact changed modes (it might have been in the middle of an input transfer), by checking the state of the busy and done lines.

The scanner is then set up using the DOA, DOC commands.

A complete sequence to continuously output a character would be:—

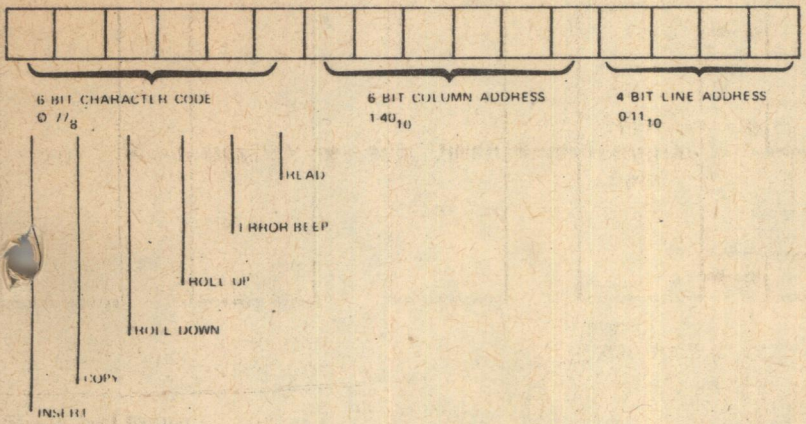
```
START   SKPDN SCNR      Is scanner already outputting?
        JMP. – 1        Yes.
        NIOP SCNR       Stop scanner.
        SKPBZ SCNR      Is scanner in Output Idle?
        JMP. – 2        No, stop again.
        DOA Ø, SCNR     Output terminal number.
        SKPBZ CHNL      Is this terminal busy?
        JMP. – 1        Yes. Wait.
        DOA 1, CHNL     Output character, column, line.
        DOCS2, CHNL     Output line, interpret and start.
        JMP START
```

ACØ:

```
        DOA Ø, SCNR.    Bits 1Ø–15 of ACØ contain the terminal
                        number.
```

AC1:

```
        DOA 1, CHNL.    AC1 has the following format:—
```

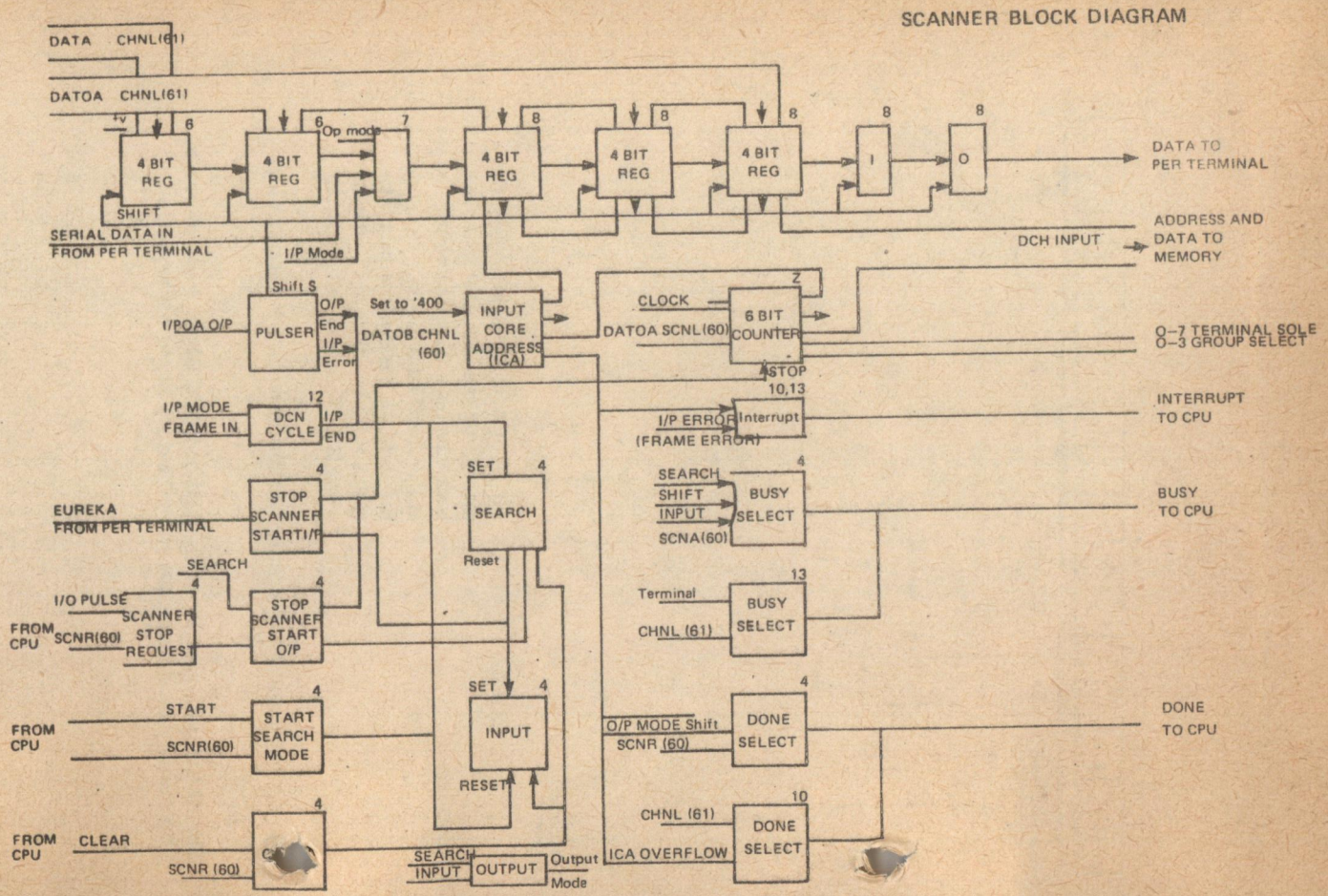


AC2:

DOLS2, CHNL. Bit 14 of AC2 is the line bit which means that the character specified is written on the whole line starting at the specified position.
Bit 15 of AC2 is the interpret bit. If this is set bits 0—5 of the previous word (AC1) are used as commands.

The start pulse included with the last command puts the scanner into Output Shift.

The 18 bits outputted in the DOA 61 and DOC 61 are made up into a 20 bit word with 2 frame bits and shifted serially to the terminal.


SCANNER BLOCK DIAGRAM
DATA CHNL(61)
DATOA CHNL(61)
+v
6
4 BIT REG
SHIFT
SERIAL DATA IN FROM PER TERMINAL
6
4 BIT REG
Op mode
7
I/P Mode
4 BIT REG
8
4 BIT REG
8
4 BIT REG
8
I
8
O
8
DATA TO PER TERMINAL
ADDRESS AND DATA TO MEMORY
DCH INPUT
Shift 5
I/POA O/P
PULSER
O/P End
I/P Error
Set to '400
DATOB CHNL (60)
INPUT CORE ADDRESS (ICA)
CLOCK
DATOA SCNL(60)
7
6 BIT COUNTER
STOP
0–7 TERMINAL SOLE
0–3 GROUP SELECT
I/P MODE
FRAME IN
12
DCN CYCLE
I/P END
10,13
I/P ERROR (FRAME ERROR)
Interrupt
INTERRUPT TO CPU
EUREKA FROM PER TERMINAL
4
STOP SCANNER START I/P
SET
4
SEARCH
Reset
SEARCH
4
BUSY SELECT
SHIFT
INPUT
SCNA(60)
BUSY TO CPU
SEARCH
I/O PULSE
SCANNER STOP REQUEST
FROM CPU
SCNR(60)
4
STOP SCANNER START O/P
Terminal
CHNL (61)
13
BUSY SELECT
SET
4
INPUT
RESET
START
FROM CPU
SCNR(60)
4
START SEARCH MODE
O/P MODE Shift
SCNR (60)
4
DONE SELECT
DONE TO CPU
FROM CPU
CLEAR
SCNR (60)
4
SEARCH
INPUT
OUTPUT
Output Mode
CHNL (61)
ICA OVERFLOW
10
DONE SELECT

PERTERMINAL CAGE

The per-terminal cage has 32 slots. For each terminal on the system there must be a card in the appropriate slot.

A Card

There is one A card for each group of 8 cards. A separate line from the scanner board selects each of the 4 groups and the low order 3 bits are sent to every A card. The A card must be in slot 1, 9, 17, or 25. The A card decodes the 3 bits and sends a select line to the other 7 cards in the group.

B Card

The B card contains no decode logic but contains all the terminating resistors for the command lines from the scanner. There is only 1 B card in each per-terminal cage which can be in any slot except an A card slot.

C Card

The C card contains no decode logic and no terminating resistors and is used for the remainder of the slots.

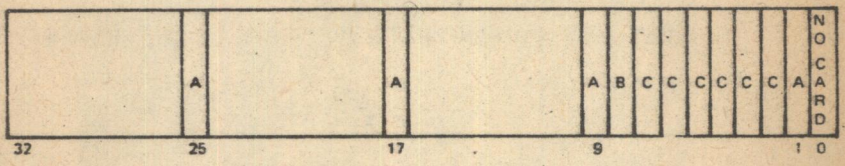
Common functions

Each card receives data from the scanner board and if its select is true (from A card) transmits the data to the terminal. Both the true and bar of the signal are sent to the terminal down the two lines of a twisted pair. This is to give noise immunity and is sensed at the other end by a differential line receiver.

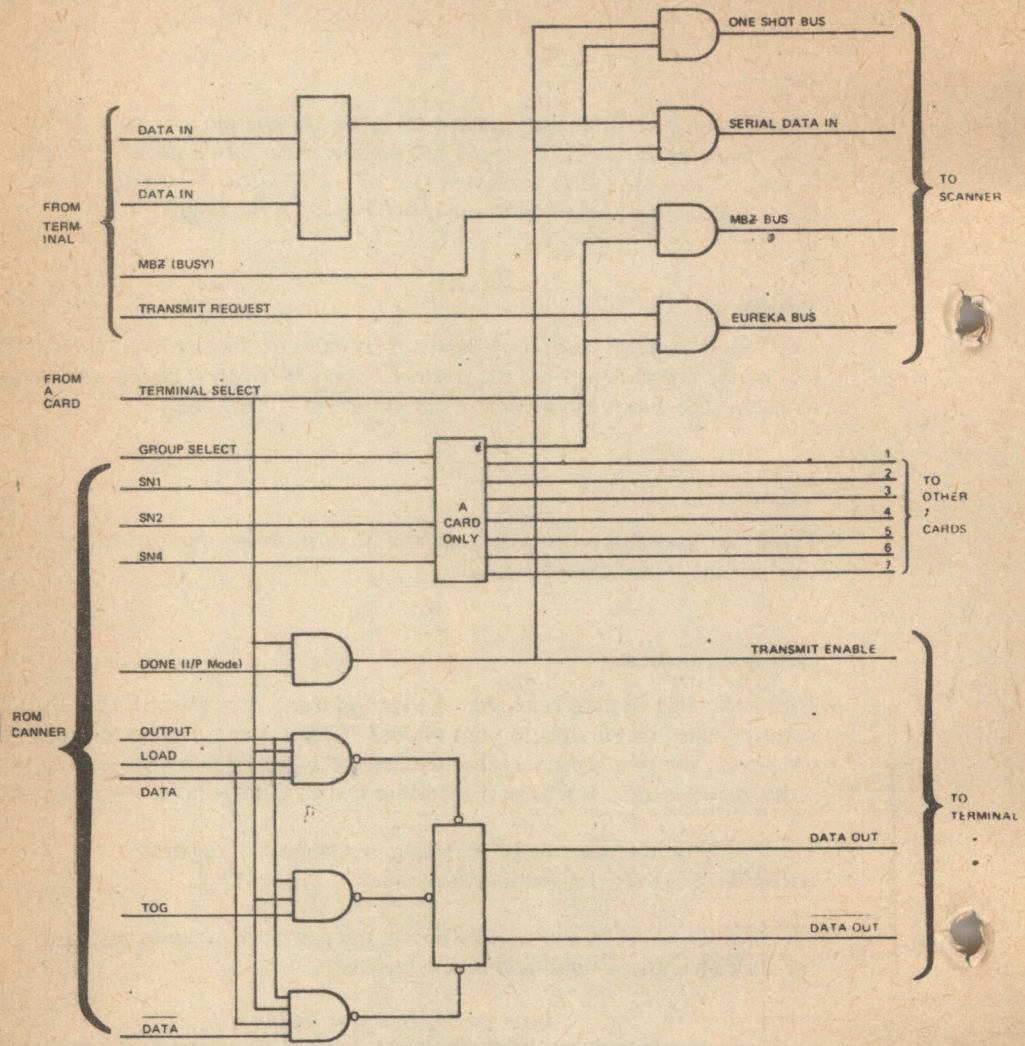
The data from the terminal is received in a differential Receiver and transmitted as a logic signal to the scanner.

All control is done by the scanner board, the per-terminal cards passing the data on without holding it in any register.

VIEW OF CARDS FROM FRONT



DIFFERENTIAL RECEIVER



KEYPUNCH KEYBOARD LOWER SHIFT	KEYPUNCH KEYBOARD UPPER SHIFT	TYPEWRITER KEYBOARD LOWER SHIFT	TYPEWRITER KEYBOARD UPPER SHIFT	CODE	SCREEN OUTPUT
X	?	Ø	)	00	Space
Z		1	+	01	A
S	>	2	@	02	B
A		3	#	03	C
W		4	S	04	D
Q	‾	5	%	05	E
@	#	6	¢	06	F
%		7	&	07	G
V	=	8	*	10	H
C	'	9	(	11	I
F	:	–	–	12	¢
D	:	.	.	13	.
R	c	P		14	<
E	)	;	:	15	(
*	S	/	?	16	+
		I		17	↑
SPACE		SPACE		20	&
B	'	Q		21	J
H	'	W		22	K
G	¬	E		23	L
Y	I	R		24	M
T	≠	T	≠	25	N
		Y		26	O
		U	1	27	P
N	(	L		30	Q
M	7	A		31	R
K	5	5	>	32	!
J	4	D	<	33	S
I	2	F		34	*
U	I	G	¬	35	)
	Ø	H	'	36	;
		J		37	¬
Function KEYS		Function KEYS			
NUM		SHIFT		1	
ALPHA				2	
PGM		PGM		4	
RCD		RCD		5	
FLD		FLD		6	

KEYPUNCH KEYBOARD LOWER SHIFT	KEYPUNCH KEYBOARD UPPER SHIFT	TYPEWRITER KEYBOARD LOWER SHIFT	TYPEWRITER KEYBOARD UPPER SHIFT	CODE	SCREEN OUTPUT
,	8	,	,	40	
..	9	Z		41	;
L	6	X		42	S
O	3	C	"	43	T
P	&	V		44	U
		B	'	45	V
		M		46	W
				47	X
		O		50	Y
		K		51	Z
				52	/
				53	.
				54	"
				55	←
				56	>
				57	?
				60	Ø
AUTO				61	1
RESET				62	2
INS				63	3
DEL				64	4
DUP				65	5
				66	6
HELP				67	7
				70	8
COR				71	9
				72	
FIELD RELEASE				73	#
→				74	"
←				75	
LOC RET				76	
REL				77	"

SEECHECK KEYSTATION

INPUT AND OUTPUT CODES

PAPER TAPE READER/PUNCH

PAPER TAPE READER/PUNCH SYSTEM

The Reader/Punch system consists of a Reader/Punch controller board 048–433–1, a G.N.T. Tape Punch model 3406 and one of the following interface compatible Tape Reader units:–

Trend U.D.R. model 350
Trend U.D.R. model 700
Trend H.S.R. model 500

The controller board is a modified version of DCC controller and contains separate control logic circuits for the Tape Punch and the Reader units. These control circuits are independent of each other and have their own individual device enable codes. These device codes are as follows:–

(1) Tape Reader – Octal 12
(2) Tape Punch – Octal 13

The controller board also contains I/O Bus driver and receiver circuits which are common to both Reader and Punch units.

Reader Control

Since the Tape Reader transmits negative logic signal and the controller requires positive logic signal, an inverter board is incorporated at the reader end of the interconnecting cable in order to make the reader and the controller compatible to each other.

To read one frame a start pulse is issued to the reader controller from the C.P.U. This clears 'Done' and sets 'Busy'. 'Busy' sets 'Go' which gives 'FWD' to the reader via pin A47 on the backplane of the B.C.G.

When the reader sees 'FWD' it moves the paper tape right to left until it finds a sprocket hole. When a sprocket hole is found 'SPKT' is sent to the controller in parallel with the eight data bits from the paper tape frame of that sprocket hole. 'SPKT' arrives at the controller on pin A77 and in a delayed form produces read strobe which clears 'Go' and 'Busy' and sets 'Done'. 'Done' enables interrupt requests provided mask bit 11 has not been used to disable it. 'Done' also clocks the data from the cable interface into a holding register. A 'DIA' to the reader will gate the data from the holding register onto the I/O bus lines from bits 8 to 15. The data remains in the holding register until replaced by further data from the reader. The paper tape will run continuously without hesitation between the frames provided all the following conditions are satisfied:–

1. C.P.U. is not too 'busy'.
2. C.P.U. checks reader 'Busy' or 'Done' frequently.
3. C.P.U. sends a start pulse promptly.

If a start pulse is not issued the tape will stop before coming to the next frame.

Punch Control

To punch one frame a 'DOA' is sent to the controller which takes the least significant 8 bits from the bus lines and thereby from the selector register and clocks them into a holding register. A start pulse will now set 'Busy' and clear 'Done'.

'Busy' triggers a monostable the output of which gates the data into the holding register via the mini backplane to the punch and also provides the 'Feed Hole' signal which activates the punch and strobes in the data.

When the operation in the punch is complete the O.K. to send more data is sent back to the controller in the form of 'Punch Feed' which is taken from pin B23 of the edge connector via a wire link to the clock inputs of the 'Busy' and 'Done' flops and so clears 'Busy' and sets 'Done'. 'Done' will enable 'Interrupt Request' but Seecheck Software normally disables it by the use of interrupt mask bit 13.

The output gates (I.C.s 1 and 25) were originally 7438's in the DCC controller board and these gates have been changed to 7408's to affect an inversion of the data to suit the particular punch unit (G.N.T. Model 3406). To get the inversion on the 'Feed Hole' signal pins 1 and 2 of I.C.50 are disconnected from pin 8 of I.C. 49 by a track cut and connected instead to pin 6 of I.C. 49 by a wire link. It is also for reasons of compatibility that 'Busy' and 'Done' are clocked directly from the interface instead of via the monostable on I.C.49.

NOTE

The reader punch controller board also contains logic circuit for teletypewriter option and a track for real time clock. These options are not currently used.